FPGA & VHDL Programming

Hardware Description Language (HDL)

By

Dr. P. S. Jadhav

What Is a Hardware Description Language (HDL)?

- ✓ Hardware description languages allow you to describe a circuit using words and symbols i.e. in textual format
- ✓ then development software can convert that textual description into configuration data
- ✓ Configuration data loaded into the FPGA in order to implement the desired functionality.

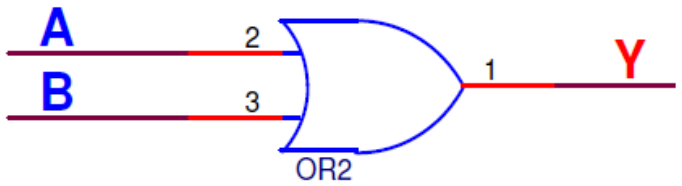
OR Gate: A logic gate whose output is logic ‘0’ if and only if all of its inputs are logic ‘0’.

Truth table

Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Y = A **OR** B
= A + B

Logic diagram

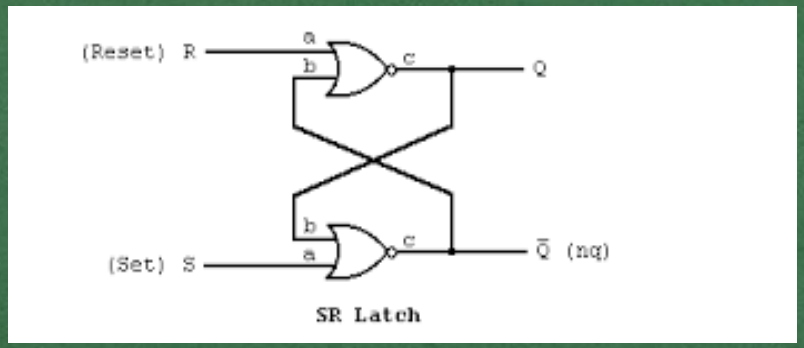



```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_arith.all;
use IEEE.std_logic_unsigned.all;
--------------------------------- Entity Declarations ------------------------
entity orgate is
Port(       A : in std_logic;
            B : in std_logic;
            Y : out std_logic
);
end andgate;
architecture Behavioral of orgate is
begin
Y<= A or  B ;
end Behavioral;
```

Why HDL's are used ?

- a digital circuit can be represented by means of interconnected diagrams.

  It is called as schematic.



SR Latch

- but it becomes impractical as complexity increases.
- Therefore Another way can be used to describe digital circuits that is HDL's
- HDL is textual language that is specifically intended to clearly and concisely capture the defining features of digital design.

Hardware description languages

- HDL is a language that describes the hardware of digital systems in a textual form.
- It resembles a programming language, but is specifically oriented to describing hardware structures and behaviors.
- The main difference with the traditional programming languages is HDL's representation of extensive parallel
- operations whereas traditional ones represent mostly serial operations.
- The most common use of a HDL is to provide an alternative to schematics.
- HDL can be used to represent logic diagrams, Boolean expressions, and other more complex digital circuits.

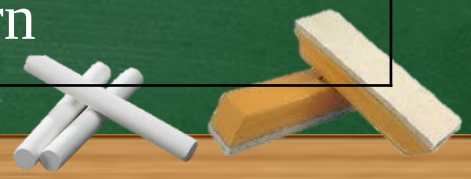
Hardware description languages

There are two standard HDL's that are supported by IEEE

1. **VHDL** (*Very-High-Speed Integrated Circuits Hardware Description Language*) - Sometimes referred to as VHSIC HDL, this was developed from an initiative by US. Dept. of Defense.
2. **Verilog HDL** – developed by Cadence Data systems and later transferred to a consortium called *Open Verilog International* (OVI).

VHDL Vs Verilog

VHDL	Verilog
Strongly typed	Weakly typed
Easier to understand	Less code to write
More natural in use	More of a hardware modeling language
Wordy	Brief or short
Non-C-like syntax	Similarities to the C language
Variables must be described by data type	A lower level of programming constructs
Widely used for FPGAs and military	A better grasp on hardware modeling
More difficult to learn	Simpler to learn



Genesis of VHDL

- During 1980s ,the rapid advances in integrated circuit technology provoked the idea of developing a standard design procedure for digital circuits .
- The VHSIC Program launched in 1980 was an initiative of the Defense Department of US to push the state of the art in VLSI technology, and VHDL was proposed as a versatile hardware description language.
- Woods Hole Workshop Held in June 1981 in Massachusetts.
- In July 1983, a team of Intermetrics , IBM and Texas Instruments were awarded a contract to develop VHDL

- In August 1985, the final version of the language under government contract was released: VHDL Version 7.2
- In December 1987, VHDL became IEEE (Institute of Electronics and Electrical engineering) Standard 1076-1987 and in 1988 an ANSI standard
- In September 1993, VHDL was restandardized to clarify and enhance the language (IEEE Standard 1076-1993)
- VHDL has been accepted as a Draft International Standard by the IEC (International Engineering Consortium)
- VHDL 1993, 1997, 2000, 2002 …

VHDL Vs Conventional Programming Language

- VHDL is inherently parallel

Commands are executes concurrently and executed as soon as new input arrives.

- Mimics the behavior of physical usually digital system
- Allows incorporation of timing specification (gate delays) as well as to describe the system as interconnection of different component
- Conventional languages are mainly used for computation, data manipulation and execution on specific hardware model
- VHDL can be used for simulation, synthesis and verification
- In a VHDL ,system can be described in four different point of view

1) behavioral 2) structural

3) Functional 4) physical properties

Related VHDL Standards

1076.1–1999: VHDL-AMS (Analog & Mixed-Signal Extensions)

1076.2–1996: Std. VHDL Mathematics Packages

1076.3-1997: Std. VHDL Synthesis Packages

1076.4-1995: Std. VITAL Modeling Specification (VHDL Initiative Towards ASIC Libraries)

1076.6-1999: Std. for VHDL Register Transfer Level (RTL) Synthesis

1164-1993: Std. Multi-value Logic System for VHDL Model Interoperability