# FPGA based Data Acquisition System for Machine Tool Spindle

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Abstract:- This article presents implementation of FPGA based data acquisition system to measure the temperature of spindle of a machine tool. Field Programmable Gate Array (FPGA) is the heart of the system which is configured and programmed to obtain real time temperature of spindle machine tool using temperature sensor IC LM-35. In order to acquire analog to digital data (ADC), Serial peripheral Interface (SPI) communication protocol has been used. The data acquisition system is designed and developed using quartus II version 15.1 and implemented on Cyclone IV E FPGA device. The measured output is stored on PC and plotted using MATLAB software.

*Keywords:*- *FPGA*; *data acquisition;*, *Altera Cyclone IV E;*, *Quartus* 

# I. INTRODUCTION

The machine tool spindle affects the performance of machine and the flexibility of the production system. As the spinning speed of spindle increases its temperature increases and when cutting speed increases then also temperature increases. Therefore to manufacture product with high precision, accuracy, good quality, it is essential to record the temperature of spindle.

In the scientific and technological research and industrial production, a variety of parameters such as sound, temperature, pressure etc. are often needed to be collected and processed. The physical data of parameters is in analog form. In the digital domain of Electronics to handle data using processor one has to convert the analog data in digital form so that processor can read, interpret and manipulate the data. The DAQ system samples signals and measures an analog physical quantity converts them into digital quantity that can be understood, measured, processed by digital device and provide output in analog form [1]. A DAQ system plays imperative role in process control, data detection, and data acquisition. Earlier different data acquisition systems have been estimated with different functionalities, Methodologies and cores. Literature reveals that microprocessors, microcontrollers, and DSP platform can be employed for developing the data acquisition system. These devices have slower speed, insufficient on-chip memory and do not allow flexibility for the user in configuring devices according to the requirement due to the hardware configuration [2].

As in [3] data acquisition system on embedded PC/104 framework has been designed and developed. A system designing criteria is to deal with the existing data acquisition system of Aditya Tokamak for plasma diagnosis which has

MDSPlus and Matlab interface. The interface and control logic have been implemented by using VHDL on CPLD (Complex programming language) [3]. DAO system using Xilinx Virtex- II Pro FPGA has been implemented. They have used both power PC and MicroBlaze processor for developing the network based controller [4]. FPGA based systems allows the hardware/software co-design. It improves significantly the system performance by providing the less time delay among the simulation and response. This coevolutionary co-operation is used to increase the computing speed of the system [5][6]. The most commonly measured environmental quantity is temperature. This is understandable given that temperature affects nearly all physical, electrical, chemical, mechanical, and biological systems. Certain chemical reactions, biological activities, and even electronic circuits work best when temperatures are kept within a specific range. Control systems that keep temperature within prescribed limits are frequently utilized when these processes need to be optimized [7]. IC sensors have been accustomed to measure the temperature, since it has good linearity, wide power range, and are small and easy to install so that no compensating circuit is needed. It is able to test a temperature range from 55°C-150°C [8].

### II. DATA ACQUISITION SYSTEM

FPGA based DAQ is designed and developed to observe and collect the spindle temperature. DAQ system includes machine tool spindle unit. The spindle temperature has been monitored using temperature sensor. The temperature data is digitized using ADC ADS 7841 with FPGA Processor. Further the temperature data has been sent to the PC through serial communication using RS 232 Protocol. The recorded data is in text form and sampling rate is 1 second. The temperature status of spindle is monitored from LED's on the FPGA Board. The LED's represents the binary value of recorded temperature also it is displayed and stored on PC in decimal value. The system is portable. *"Fig.1"* displays FPGA Based Data Acquisition System.

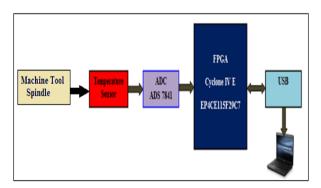


Fig. 1: FPGA Based Data Acquisition System

### III. SYSTEM COMPONENT

#### A. Machine Tool Spindle

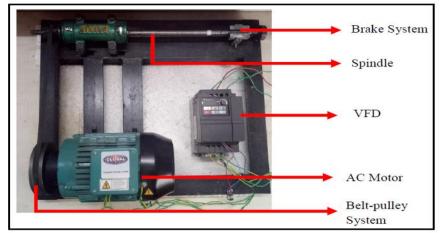


Fig. 2: Machine Tool Spindle Unit

As in "*Fig 2*". The spindle is externally driven by the motor using belt pully system. Variable Frequency Drive (VFD) has been used to obtain variable speed of spindle. The rotational speed (rpm) of spindle is measured by using non-contact tachometer. In the present system load is not present, hence braking system is designed to apply radial friction on spindle. As the rotational speed increases temperature of spindle increases. Therefore with applied friction heat will be generated. Temperature of spindle has been measured using data acquisition system.

### B. Temperature Sensor

The analog IC sensor LM-35 is used to measure the temperature, since it has good linearity, wide power range, and is small and easy to install. It can measure the atmosphere temperature around it or machine tool temperature to which it is connected or the human body temperature. The LM35 are precision integrated-circuit

sensors, whose analog output voltage is comparative to the temperature in centigrade. It operates from  $55^{\circ}$  C to  $100^{\circ}$ C. Its scale factor is  $10 \text{ mV/}^{\circ}$  C (millivolt per degree centigrade) and output is in range from 0 V to 5V [9]. The +5 V supply is applied to the temperature sensor direct from the FPGA board and output is given to the ADC.

### C. ADC ADS7841

The ADC ADS 7841 is a 12 bit sampling successive approximation ADC with 4 channels. It has Serial Synchronous Interface. It operates from 2.7 Volt to 5 Volt. It is 16 pin IC and functions over temperature range of  $-45^{\circ}$ C to  $125^{\circ}$ C. It is Low power, high speed ADC and has on board multiplexer. This facility makes ADC ADS 7841 portable multichannel data logger [10]. The system make a use of SPI in which ADC ADS 7841 works as slave where as FPGA acts as Master. The connections required by ADC ADS 7841 are as in "*Fig 3*".

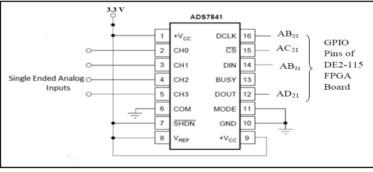


Fig. 3: Pin Connection of ADC

### D. Processing Unit

The processing unit is Altera Cyclone IV E EP4CE115F29C7 (DE2-115) with Nios-II Processor. DE2-115 FPGA development board is displayed as in "*Fig.4*". It contains cyclone <sup>@</sup>IV 4CE115 FPGA device and the Serial Device EPCS64. It supports Active Serial Programming (AS) and JTAG. The USB Blaster for programming is

available. The 50 MHz clock is available and external clock can be applied. It has 40 general purposes I/O (GPIO) Pins. It has 114,480 logic elements. In this system GPIO works on 3.3 V. The programming has been performed by using Quartus II Software. The FPGA GPIO pins are utilized for interfacing with ADC [11].

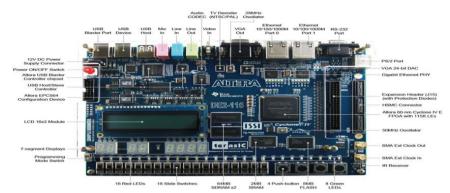


Fig. 4: DE2-115 FPGA Development Board

#### E. Computer/PC

Computer/PC is used to visualize the output of application. The real time temperature response of spindle of a machine tool is observed on PC with the terminal emulator software.

#### IV. HARDWARE- SOFTWARE CO-DESIGN IMPLEMENTATION

It is performed by Altera Qsys Builder existing in the Quartus II prime edition 15.1. The Qsys Builder is system integration tools that save time and exertion in the design process by connecting IP functions and subsystems. The desired system is implemented merely by selecting the required components as processor core, memory, I/O ports and stating the parameters required for the system using Qsys Builder. The Qsys tool let the users to utilize already available and/or custom components for system development. After interconnecting components the design is downloaded into the FPGA board. The system is reduced with the use of Qsys tool. The errors get reduced, debugged easily and performance is optimized because of this small system. The system generated by Qsys tool contains VHDL code of each element and structure [12].

□ onchip_memory2_0	On-Chip Memory (RAM or ROM)			
♦ dk1	Clock Input	Doub clk_0		
s1	Avalon Memory Mapped Slave	Doul [dk1]	© 0x0000_0000	0x0003_1fff
reset1	Reset Input	Doul [dk1]		
□ Input_1	PIO (Parallel I/O)			
♦ dk	Clock Input	Doub clk_0		
◆ ◆ ◆ reset	Reset Input	Doul [dk]		
◆ ◆ → s1	Avalon Memory Mapped Slave	Doub[dk]		0x0000_000f
external_connection	Conduit	Doul		
	PIO (Parallel I/O)			
♦ dk	Clock Input	Doul clk_0		
	Reset Input	Dout [dk]		
	Avalon Memory Mapped Slave	Dout [dk]		0x0000_000f
	Conduit	Doul		
Output_1	PIO (Parallel I/O)			
♦ dk	Clock Input	Dout clk_0		
♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦ ♦	Reset Input	Dout [dk]		
	Avalon Memory Mapped Slave	Dout [dk]	© 0x0000_0000	2000_000x0
	Conduit	Dout		
🗆 uart_0	UART (RS-232 Serial Port)			
♦ dk	Clock Input	Doul clk_0		
	Reset Input	Doul [dk]		
	Avalon Memory Mapped Slave	Dout [dk]		0x0000_001f
	Conduit	Dout		
	Interrupt Sender	Dout [dk]		

Fig. 5: System Component, Connections with base addresses

After selecting and specifying the all desired system components for the implementation ("*Fig 5*".), the system is generated. The specified system is saved by the name 'ADS', then the VHDL code generated by clicking generate option as displayed in "*Fig 6*".

💑 Generation					
▼ Synthesis					
Synthesis files are used to compile the system in a Quartus Prime project.					
Create HDL design files for synthesis: VHDL 👻					
Create timing and resource estimate	ates for third-party EDA synthesis tools.				
Create block symbol file (.bsf)					
<ul> <li>Simulation</li> </ul>					
The simulation model contains genera	ted HDL files for the simulator, and may include simulation-only features.				
Simulation scripts for this component	will be generated in a vendor-specific sub-directory in the specified output directory.				
Follow the guidance in the generated simulation scripts about how to structure your design's simulation scripts and how to use the <i>ip-setup-simulation</i> and ip-make-simscript command-line utilities to compile all of the files needed for simulating all of the IP in your design.					
Create simulation model: None 👻					
Allow mixed-language simulation					
Enable this if your simulator supports	mixed-language simulation.				
* Output Directory					
Path:	C:/Users/Poonam/Desktop/VHDL				
L	Generate Cancel				

Fig. 6: VHDL Code Generation

After VHDL code generation Qsys system integrated into Quartus II project, implements hardware modules into the FPGA design. Here pin locations are assigned, timing requirements are assigned and other design constraints are applied. Then the hardware design compiled for target board. For Implementation of application on FPGA board .sof file is created. After running the program the result is displayed on FPGA Board and stored on PC ("Fig.7") for further processing.



Fig. 7: Temperature Measurement of Machine Tool Spindle

# V. RESULT ANALYSIS

The complete DAQ system is implemented on Altera's Cyclone IV E FPGA Development Board. After successful compilation ("Fig.7") device utilization summary is obtained as in ("Fig.8").

Entity Instance Cyclore IV E EP4CE115F29C7	Herarday + ≡ (3) & ×	Complete Table of Contents	on Report - ADS7841 Flow Summary	۵		
Cyclore IV E. EP4CE115F29C7		Table of Contents	Fame Sammary			
			Film State	Successful - Sat May 19 19 49:50 2018		
■ Grower N E Sever 119 and C		Flow Settings Flow Non-Defaul Oxtal Settings Flow Dayset Tine Flow OS Summery Flow Log Flow Log Anthread Synthese Anthread Synthese	Quartus Prine Version Revision Name Tos-Invel Erithy Name Family Device Toming Blocks Total light cements Total combinations functions	15.15-864-1155 IOS12015 53 Steward Edites ADDTes1 ADD BV4CCTS2027 FM8 1.7787 11-4805 (2.%) 1.7787 11-4805 (2.%)		
eks Compilation		Assenbler     Assenbler     TemOvest Timing Assence:	Deboter type registre         502           Train registre         502           Train registre         47           Train registre         47           Train registre         6           Train registre         15           Train registre	492		
Task	Ó Tra	B EDA Nethel Writer				
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Fitter (Plaza & Route)	00-01-02	-				
Assembler illenerate pro	commung files) (0:00-12					
TraeQuest Timing Analysis	a 00.00.19					
EDA Netist Writer	00:00:17					
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Program Device (Open Progr	amter)					
		x				

Fig.	8:	Compil	lation	Report
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Table 1: Device Utilization Report

	Used	Available	Utilization		
Total Logic Elements	1,778	114,480	2 %		
Total combinational functions	1,653	114,480	1 %		
Dedicated logic registers	952	114,480	< 1 %		
Embedded Multiplier 9-bit elements	0	532	0		
Total registers	952				
Total Pins	47	529	9%		
Total memory bits	1,648,640	3,981,312	41 %		
Total PLLs	0	4	0%		

Table 1 shows that total logic elements available are 114,480 out of which 1,778 logic elements are used that is only 2% logic elements are utilized. Out of 529 pins 47 pins

are used that is only 9% pins are utilized. Component used by this system is very less. The temperature recorded by DAQ System is given in Table 2.

Table 2. Temperature Readings of machine tool spindle						
Time(sec)	temperature	Time(sec)	temperature	T ime(sec)	temperature	
	of spindle		of spindle		ofspindle	
	്ന		്ന		്ര	
0	28.32	280	30.27	560	31.25	
10	28.32	290	30.76	570	31.74	
20	28.32	300	29.79	580	31.74	
30	28.32	310	30.27	590	31.74	
40	28.32	320	30.76	600	31.74	
50	28.32	330	29.79	610	31.74	
60	28.81	340	30.76	620	31.74	
70	28.81	350	31.25	630	31.74	
80	29.3	360	31.25	640	31.74	
90	29.3	370	31.25	650	31.74	
100	29.3	380	30.76	660	31.25	
110	28.81	390	30.76	670	31.25	
120	28.81	400	31.25	680	31.25	
130	29.3	410	31.25	690	31.74	
140	29.79	420	30.76	700	31.74	
150	29.79	430	30.76	710	31.74	
160	29.79	440	31.25	720	31.74	
170	29.79	450	31.25	730	31.74	
180	30.27	460	31.25	740	31.74	
190	29.79	470	30.76	750	32.23	
200	29.79	480	31.25	760	31.74	
210	29.79	490	31.25	770	31.74	
220	30.27	500	31.25	780	31.74	
230	29.79	510	31.25	790	31.74	
240	30.27	520	31.25	800	31.74	
250	30.27	530	31.25	810	31.74	
260	29.79	540	31.25	820	32.23	
270	30.27	550	31.25	830	32.23	

Table 2: Temperature Readings of machine tool spindle

The system was successfully implemented for monitoring the temperature of machine tool spindle at 1000 rpm . The photograph of tested system was displayed in *"Fig.7"*. The real time temperature response of machine tool spindle has been displayed in *"Fig.9"*. The sampling rate is

of 10 sec. The temperature reading of spindle of a machine tool has been displayed in Table 2. The temperature of machine tool spindle varies from  $28.3^{\circ}$  c to  $32.23^{\circ}$  c at 1000 rpm.

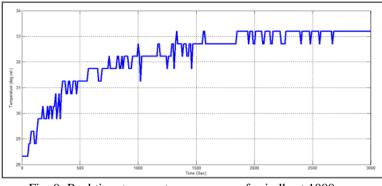


Fig. 9: Real time temperature response of spindle at 1000 rpm

# VI. CONCLUSION

In conclusion, the temperature data acquisition system designed for industrial applications has proven to be a valuable asset in monitoring temperature-related processes. Through the implementation of this system, several significant findings and outcomes have been observed. This system successfully collected and recorded real-time temperature data from the machine spindle tool with high accuracy and precision. This enabled the identification of temperature patterns providing valuable insights into the performance of industrial processes. In this FPGA based data acquisition system minimum off-board components are used. FPGA-based DAQ system provides a powerful and flexible solution for industrial applications that require highspeed data acquisition, precise synchronization, and realtime processing. With the ability to handle large data volumes, accommodate various sensors, and offer low latency and power consumption, this system plays an important role in enabling advanced data-driven decision-making, control and optimization in industrial settings.

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