"Dissemination of education through Knowledge, Science and Culture"
-Shikshanmaharshi Dr. Bapuji Salunkhe

Shri Swami Vivekanand Shikshan Sanstha's
VIVEKANAND COLLEGE, KOLHAPUR
(AUTONOMOUS)

Date: 25/03/2023

Notice

(B.Sc.I Electronics)

All the students of B.Sc.I Electronics are hereby informed that they should write a **Home assignment on Unit 1-Bipolar Junction Transistor (BJT)** of total 20 marks on a full scape paper and submit to the department on or before 28/3/2023.

Q.1 Long answer questions: [8 marks]

i. Draw circuit arrangement to determine the input and output characteristics of CE configuration and explain them.

Q.2 Short answer questions: [each for 4 marks] [12 marks]

i. Define α and β? Derive the relation between them.
ii. Explain DC load line and Q-point.
iii. Explain transistor leakage currents I_{CBO} and I_{CEO}.

Dr. C. B. Patil
(Subject Teacher)

Dr. C. B. Patil
HEAD
DEPARTMENT OF ELECTRONICS
VIVEKANAND COLLEGE, KOLHAPUR
(AUTONOMOUS)

VIVEKANAND COLLEGE ESTD. JUNE 1964 KOLHAPUR-416 003

Shri Swami vivekanand Shikshan Santha's

VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

B.Sc . - I 2022-23

Analog Electronics

Assignment I :Unit -I Bipolar Junction Transistor

Sr. No.	Roll No.	Student Name	Assignment Submitted	Marks Obtained
1	7201	AWATI SHREYASH DILIP	Submitted	14
2	7204	KAMBLE SAURABH SANJAY	not Submitted	0
3	7207	LOKHANDE SUJAL SANDIP	not Submitted	0
4	7208	MANGAONKAR VEDANT PRASHANT	Submitted	20
5	7209	MISAL OMKAR SUNIL	Submitted	17
6	7210	MUJAWAR ZAHIR JAMIR	not Submitted	0
7	7211	NESARKAR SIDDHARTH DEEPAK	not Submitted	0
8	7214	PATIL HARSHAD RAJGONDA	not Submitted	0
9	7219	SHELAKE RUPALI	not Submitted	0
9	7215	PATIL HARSHVARDHAN DHANANJAY	not Submitted	0
10	7223	WARANGE NIRAJ RAJESH	Submitted	20
11	7224	YADAV HARSH NIVAS	not Submitted	0
12	7229	BHADARAGE ABHISHEK SUNIL	Submitted	20
13	7279	ALANBAGI AHMED QASIM HASAN	Submitted	15
14	7281	ASANEKAR YASH TUKARAM	Submitted	20
15	7282	BAMANE SAHIL NIVRUTI	Submitted	20
16	7283	BAVACHE SHRAVANI BHIMRAV	Submitted	20
17	7284	CHOUGULE SAI CHANDRAKANT	Submitted	20
18	7285	CHOUGULE VAIBHAVI JAYSING	Submitted	20
19	7286	DHUMALE SANIKA SANTOSH	Submitted	20
20	7287	GHUMAI DHIRAJ BABASO	not Submitted	0
21	7288	GURAV SANIKA RAVINDRA	Submitted	20
22	7289	HIRDEKAR SHREYA SHASHIKANT	Submitted	20
23	7291	KANGRALKAR GAYATRI GUNDU	Submitted	20
24	7292	KUMBHAR DIKSHA YUVRAJ	Submitted	20
25	7293	KUMBHAR PRATHMESH YUVRAJ	not Submitted	0
26	7294	KUMBHAR SANIKA SANJAY	Submitted	20
27	7296	MANE AARATI PRAKASH	Submitted	20
28	7297	MANE ADITYA SHARAD	Submitted	20
29	7299	NANAVARE ADARSH VIJAY	Submitted	20
30	7301	NIMBALKAR SAIRAJ NANDKUMAR	Submitted	20
31	7302	PARPOLKAR SANIKA SUBHASH	Submitted	20
32	7303	PATIL ADITYA MANSING	not Submitted	0
33	7304	PATIL KIRTI SAMBHAJI	not Submitted	0
34	7305	PATIL POONAM NARSU	Submitted	20
35	7306	PATIL PRADNYA PRADIP	Submitted	20
36	7307	PATIL PRATHAMESH BHAGAVAN	Submitted	20

37	7308	PATIL RAVIRAJ BAJIRAO	Submitted	20
38	7309	PATIL RIYA NITIN	Submitted	20
39	7310	PATIL SAHIL VISHNU	Submitted	20
40	7311	PATIL SAMARTH SHRIKANT	Submitted	20
41	7312	PATIL SAMMED DHANYAKUMAR	not Submitted	0
42	7313	PATIL SOURABH BHAGAWAN	Submitted	20
43	7314	PHADAKE SUMIT RAMBHAU	not Submitted	0
44	7317	SAWANT PRATHAM PRADEEP	Submitted	20
45	7318	SHETE ANUSHKA SUNIL	Submitted	20
46	7319	SURVE VIKRANT RAJENDRA	not Submitted	0
47	7320	TIWADE KETAN GIRISHKUMAR	Submitted	20
48	7325	GHODE VAISHNAVI SHRIKANT	Submitted	15
49	7332	LAMBE SANKET JAYKUMAR	Submitted	20
50	7333	LOLAGE GAYATRI GAJANAN	Submitted	0
51	7344	PATIL SHARVARI KULDEEP	Submitted	20
52	7550	DADDIKAR GAURAV NITIN	not Submitted	0
53	7551	ALTEKAR ADITYA MAHESH	Submitted	20
54	7563	AHMED SAMI ALITTIBIN	Submitted	20
55	7567	PATIL SWAPNIL SURESH	Submitted	20
56	7569	SHINDE RUGVED TANAJI	not Submitted	0
57	7584	PATIL PRATHMESH KALLAPPA	Submitted	20

Dr. C.B.Patil
Subject Teacher

Dr. C.B.Patil
Head
Department of Electronics
Vivekanand College, Kolhapur.

VIVEKANAND COLLEGE ESTD. JUNE 1964 KOLHAPUR-416 003

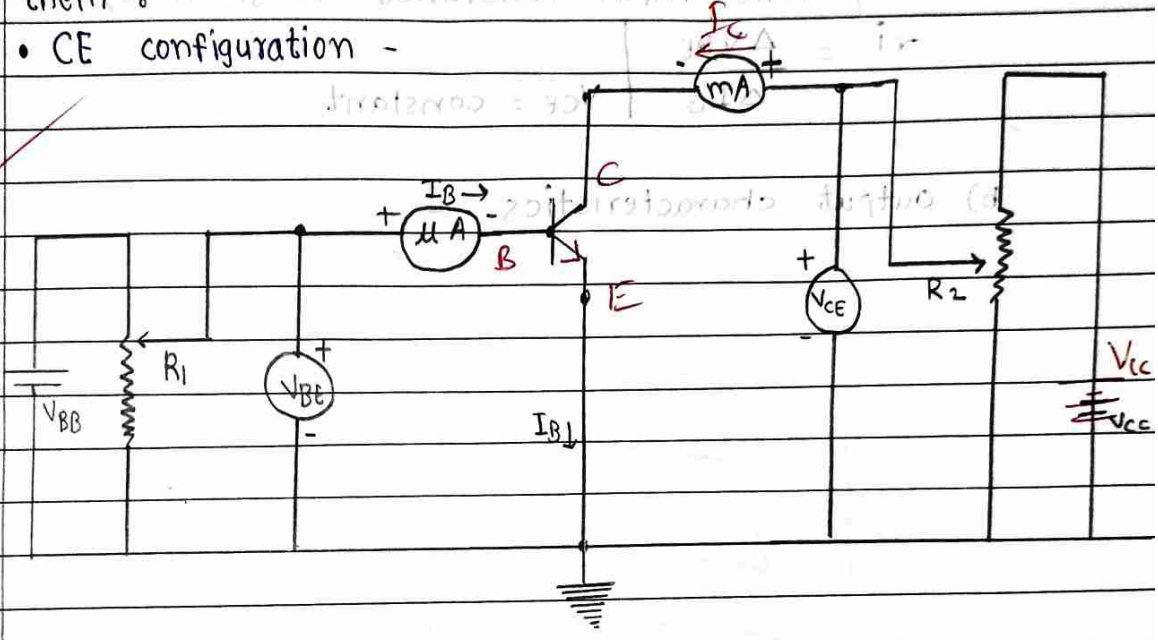
DATE PAGE NO. 20/20

Name :- Aditya Mahesh Altekar
Roll no :- 7551
Subject :- Electronics
Home Assignment

Q.1 Long Answers questions :

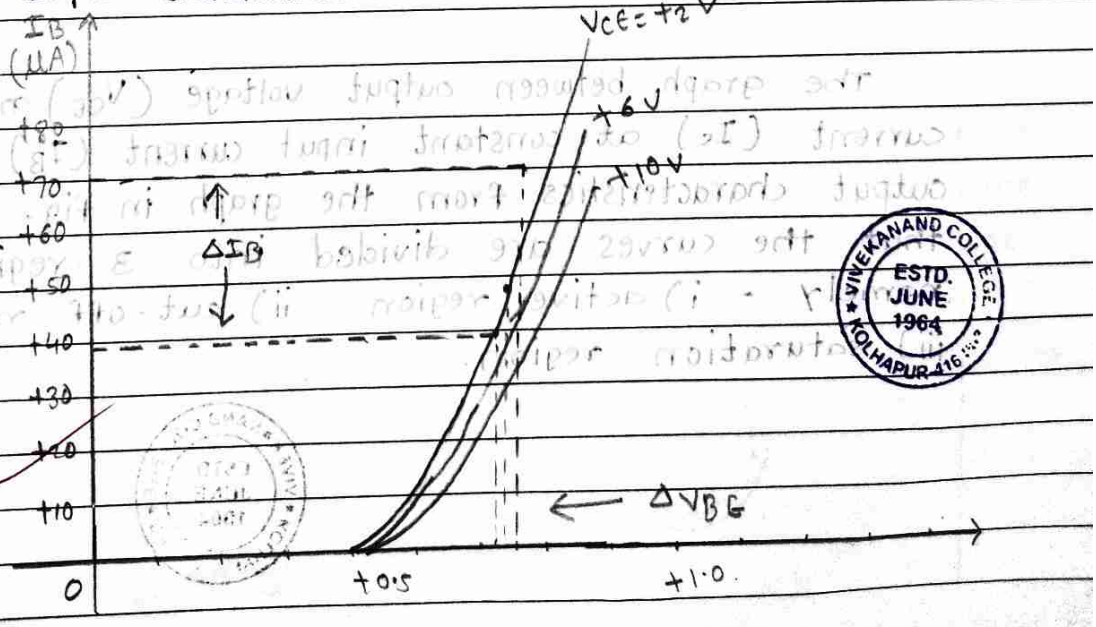
i) Draw circuit arrangement to determine the input and output characteristics of CE configuration and explain them :

• CE configuration -



The diagram shows the circuit arrangement of determining the characteristic of transistor in CE configuration

a) Input characteristic -

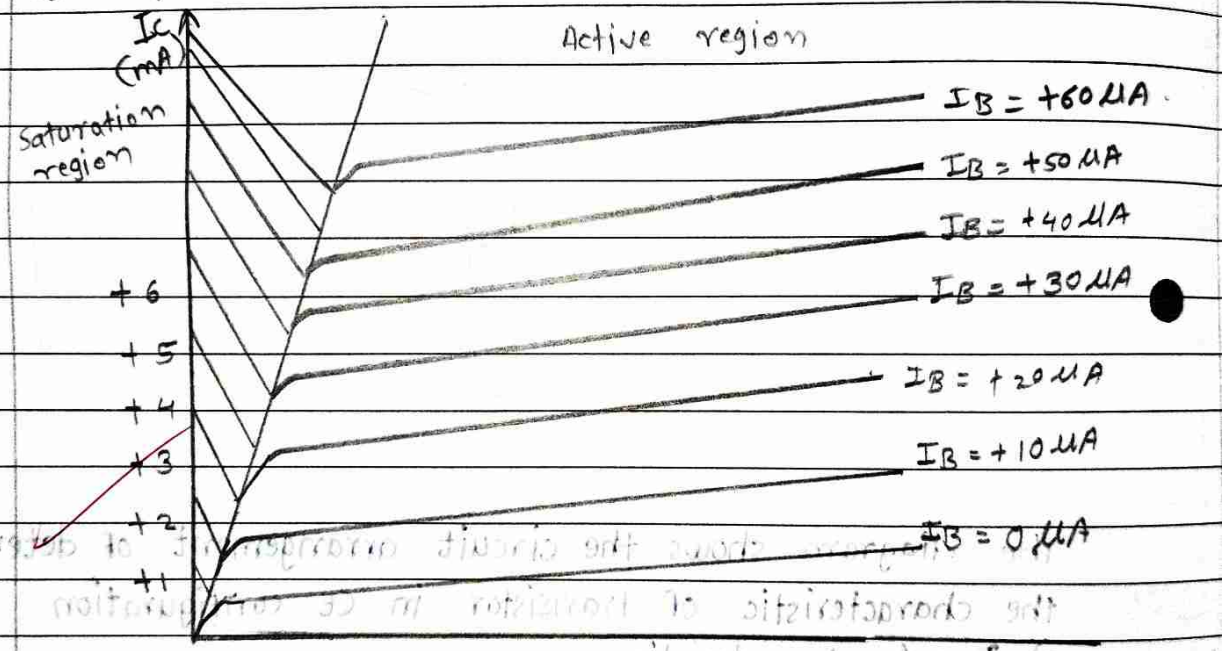


The graph between input voltage (V_{BE}) and input current (I_B) at constant output voltage (V_{CE}) is called as input characteristics. From the circuit diagram in fig. it is seen that the emitter base junction is forward biased. Hence current I_E increases exponentially with input voltage V_{BE} as shown in fig. As collector voltage increases curve shift towards the right side this is because less base current flows for the same value of V_{BE}.

The dynamic input resistance is given by

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B} \quad \Big| \quad V_{CE} = \text{constant}$$

b) Output characteristics -



The graph between output voltage (V_{CE}) and output current (I_C) at constant input current (I_B) is called output characteristics from the graph in fig. it is seen that the curves are divided into 3 regions namely - i) active region ii) cut-off region iii) saturation region.

i) Active region :-

In active region emitter junction is forward biased and collector junction is reverse biased, thus the transister operates in normal mode. As collector voltage increases, the width of depletion layer, inrese this decrease of the effective base width because of this the recombination in base region and hence the base current decreases slightly this will increase the collector current. Thus for given base current as collector voltage increases, collector current also increases and the output curves are inclined as shown in graph.

The dynamic output resistance is given by A.

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} \quad \Big| \quad I_B = \text{constant}$$

ii) cut-off region :-

The region below the curve $I_B = 0$ in fig. is known as cut-off region. In this region both junctions are reverse biased and only leakage current flows through the transistor, the tran-sistor is in cut-off state and acts as an open switch.

iii) Saturation region :-

In this region both the junctions are in the forward biased large current flows through the tranisistor and transistor acts as a close switc.

Q.2 short answers questions :-

i) Define α & β ? Derive the relation between them in C_B.

→ • DC current gain :- The ratio of the collector current I_C to emitter current I_E is called as dc current gain, denoted by α_{dc}

$$\alpha_{dc} = \frac{I_C}{I_E}$$

The value of α_{dc} is nearly equal to 1 but always less than 1 it never becomes greater than or equal to 1.

• A.C current gain :- The ratio of charge in collector current to change in emitter current at constant V_{CB} called as AC current gain. denoted by α_{ac}

$$\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E} \Big| V_{CB} = \text{constant}.$$

The value of α_{ac} nearly equal to the 1.

• DC current gain in CE :- The ratio of collector current (I_C) to base current (I_B) called DC current gain and denoted by β_{dc}

$$\beta_{dc} = \frac{I_C}{I_B}$$

• AC current gain in CE :- The ratio of change in collector current to change in base current at constant V_{CE} called as AC current gain and denoted by β_{ac}

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_E} \Big| V_{CE} = \text{constant}$$

In CE configuration, the ratio of emmitter current (I_E) to base current (I_B) is called as DC current gain, denoted by γ_{dc}

Relation between α_{dc} and β_{dc}

Since $I_E = I_B + I_C$

dividing both sides by I_C, we get

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

but, $\frac{I_E}{I_C} = \frac{1}{\alpha_{dc}}$ and $\frac{I_B}{I_C} = \frac{1}{\beta_{dc}}$

i.e. $\frac{1}{\alpha_{dc}} = \frac{1}{\beta_{dc}} + 1$

$$\therefore \frac{1}{\alpha_{dc}} = \frac{1 + \beta_{dc}}{\beta_{dc}}$$

$$\boxed{\alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}}}$$

similarly, $\frac{1}{\alpha_{dc}} = \frac{1}{\beta_{dc}} + 1$

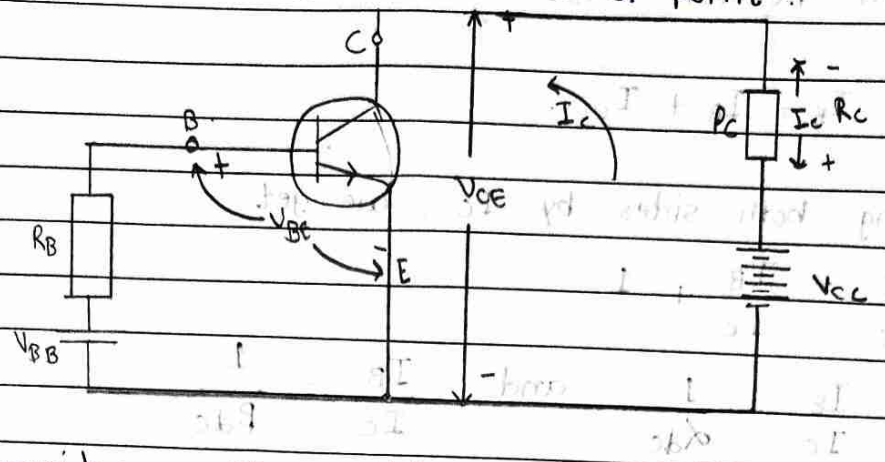
$$\frac{1}{\beta_{dc}} = \frac{1}{\alpha_{dc}} - 1$$

$$\boxed{\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}}$$

Relation between α_{ac} and β_{ac}

$$\alpha_{ac} = \frac{\beta_{ac}}{1 + \beta_{ac}} \quad \text{and} \quad \beta_{ac} = \frac{\alpha_{ac}}{1 - \alpha_{ac}}$$

ii) Explain DC load line and Q point.



consider a CE amplifier circuit without any ac input signal. This condition is called 'quiescent condition'. The battery V_{CC} sends current I_C through the load resistance R_C and the transistor.

Applying kirchhoff's voltage law the collector circuit, we get

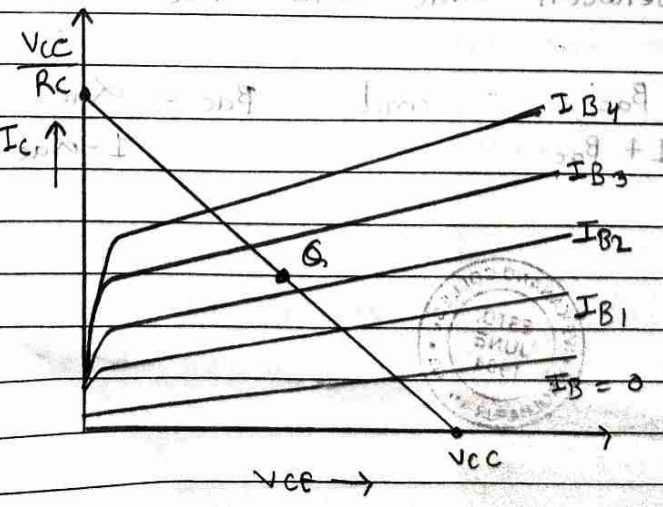
$$V_{CC} = I_C R_C + V_{CE}$$

Rearranging and solving for I_C

$$I_C = \left(\frac{-1}{R_C}\right) V_{CC} + \frac{V_{CC}}{R_C}$$

This eqⁿ is similar to $y = mx + c$ which is eqⁿ of straight line. Thus plotting eqⁿ on transistor output characteristic. we get a straight line, whose slope is $\left(\frac{-1}{R_C}\right)$ & intercept on the I_C axis is $\frac{V_{CC}}{R_C}$.

The slop of this line depends on DC load resistance RC hence called dc load line.



from eqn we have,

i) when $V_{CE} = 0$, $I_C = V_{CC} / R_C$

ii) when $I_C = 0$, $V_{CE} = V_{CC}$

joining these two points gives the dc load line as shown in graph. The dc load line intersects the output curves. The point of intersection of load line for specified base current I_B is called as 'quiescent point' or 'operating point' or 'Q point'. The exact location of q point decided by V_{CC}, R_C, R_B, V_{BE} & V_{BB} for given values of V_{CC} & R_C, the q point depends upon base current I_B, which is calculated as follows, applying kirchhoff's voltage law to the base circuit, we get,

$$V_{BB} = I_B \cdot R_B + V_{BE}$$

$$\therefore I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{V_{BB}}{R_B}$$

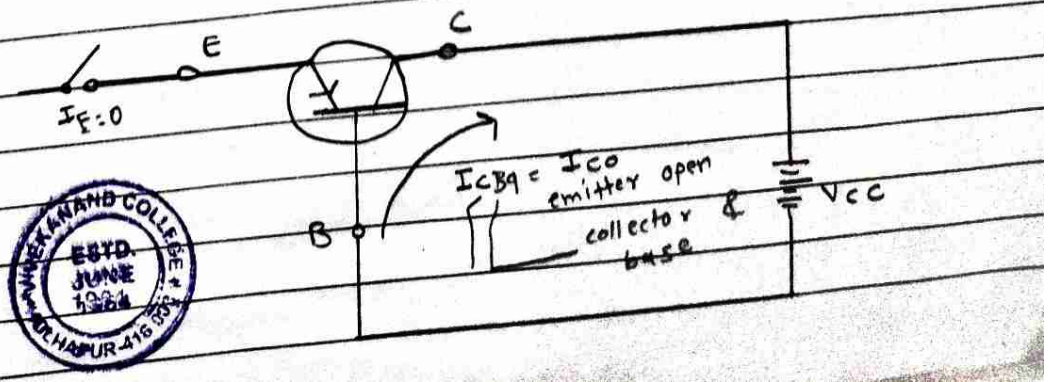
since V_{BE} is small (V_{BE} is 0.7 V for Si & 0.3 V for Ge)

iii) Explain transistor leakage current I_{CBO} and I_{CEO}

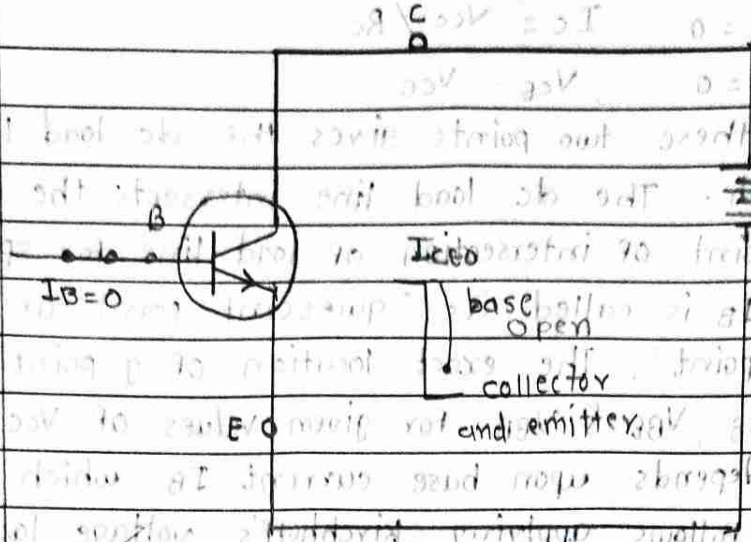
→ In CB - configuration - (I_{CBO})

if emitter terminal is open ($I_E = 0$) then only reverse saturation current I_{CO} flows through the collector circuit. This current, denoted by I_{CBO} or I_{CO}. This current is very very small, because it is due to minority charge carries. This current is temperature dependent. As temperature increases, I_{CBO} is increases. It doubles for every 10°c rise in temperature. Thus the total current is given by $I_C = \alpha I_E + I_{CBO}$

4



In CE - configuration (I_{CEO})



if base terminal is open ($I_B = 0$), then some leakage current flows through collector circuit. This current is called as collector cut-off current denoted by I_{CEO}.

Thus the total collector current is $I_C = \beta I_B + I_{CEO}$

Name - Vaishnavi Shrikant Ghode
Roll No - 7325
class - FY. BSc

15/20

Q.1 Long answer questions

i) Draw a circuit arrangement to determine the input and output characteristics of CE configuration and explain them

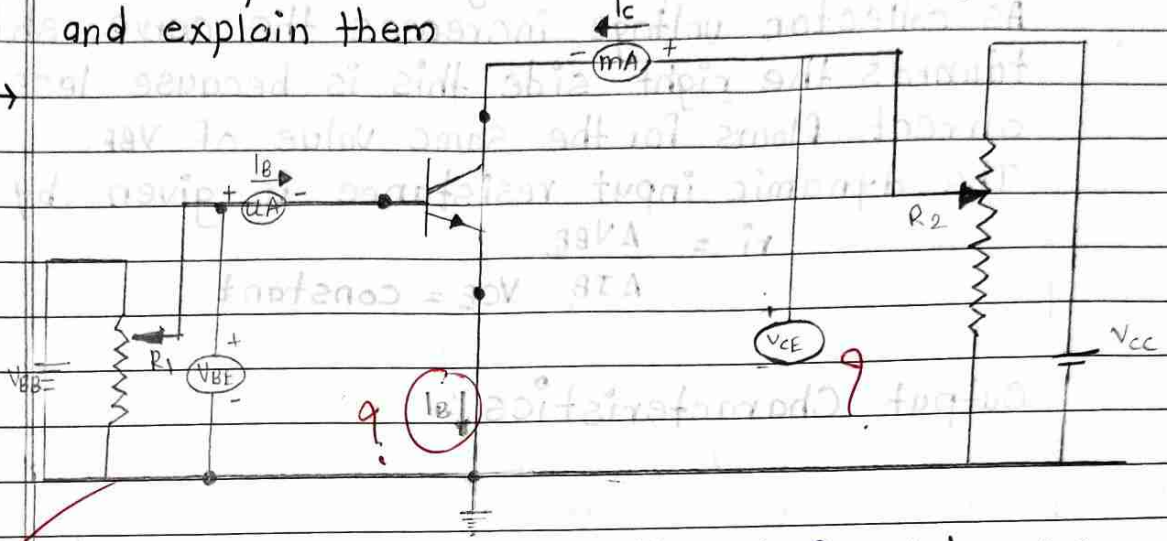
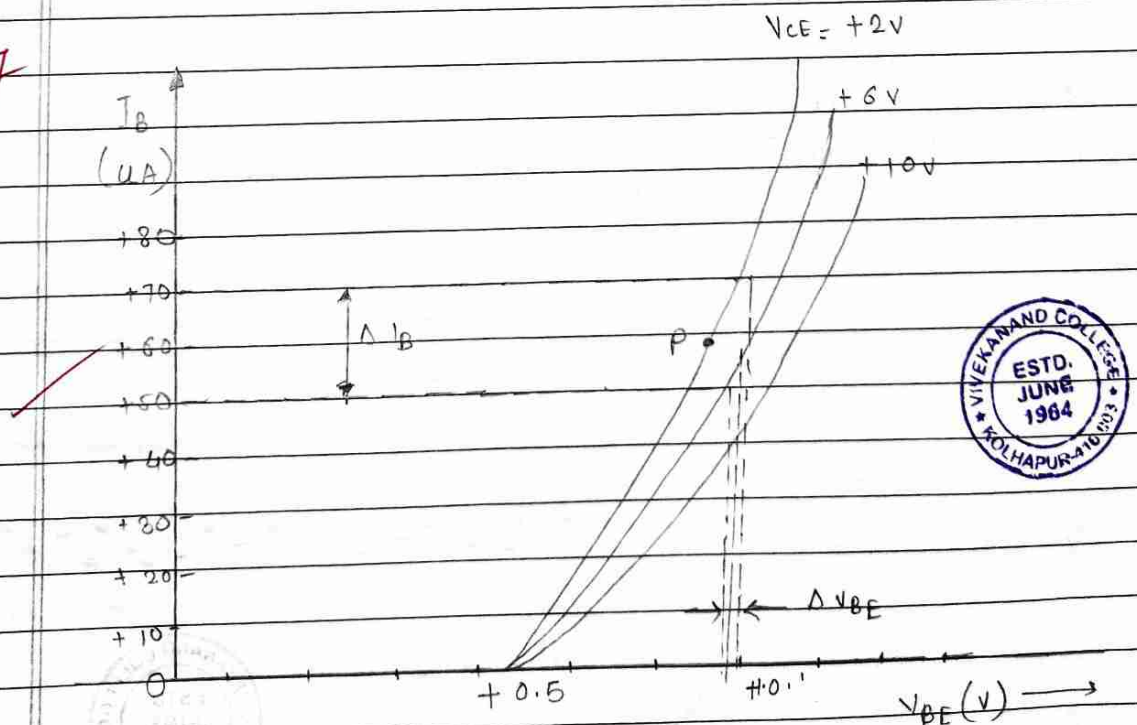


fig shows the circuit arrangement for determining the characteristics of transistor in CE Configuration

Input Characteristics

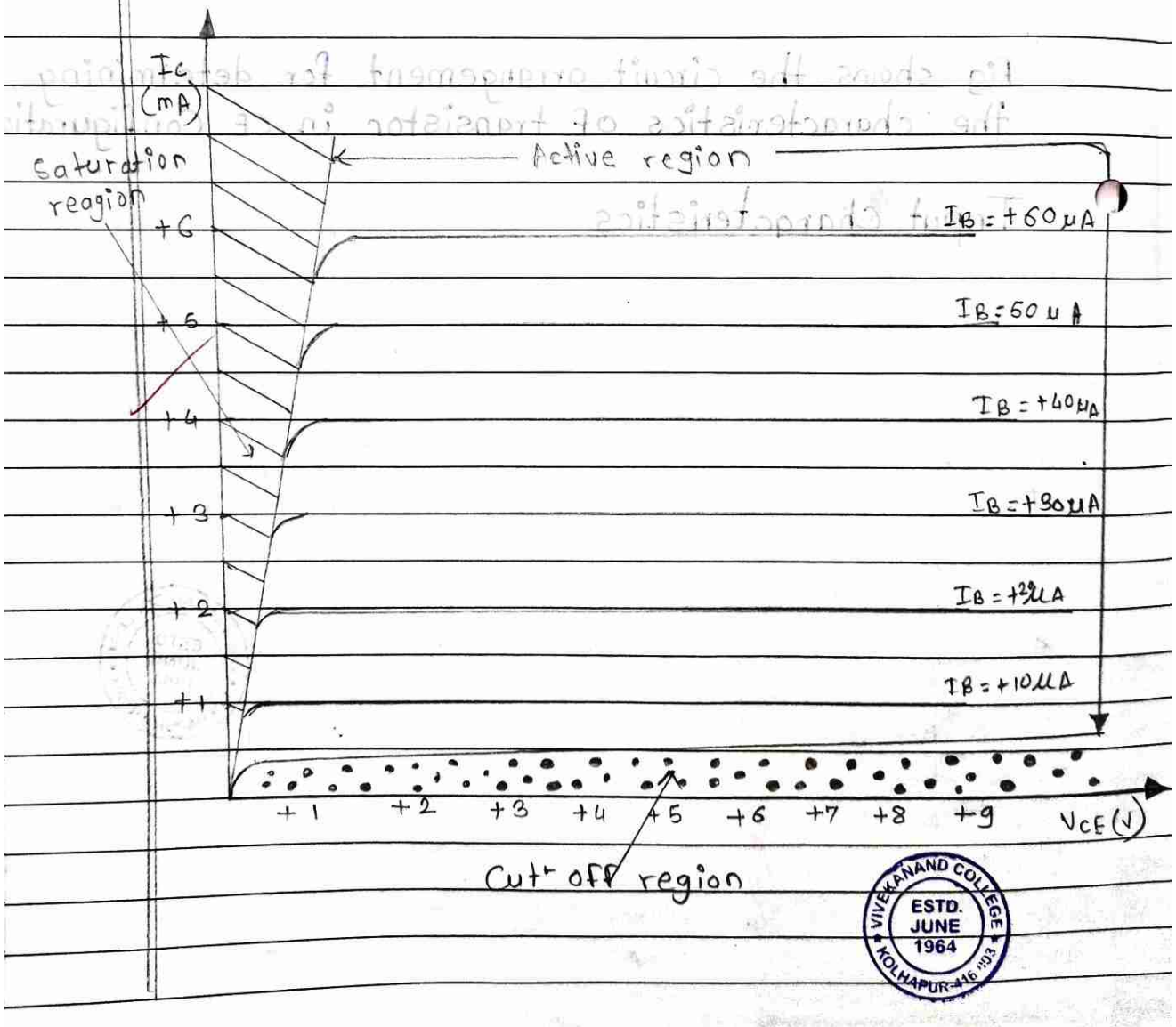


The graph between input voltage and input current at constant output voltage is called as input characteristics. From the circuit diagram in fig it is seen that the emitter base junction is forward biased. Hence current I_E increases exponentially with input voltage V_{BE} as shown in fig As collector voltage increases the curve shift towards the right side this is because less base current flows for the same value of V_{BE}.

The dynamic input resistance is given by

$$r_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$$

Output Characteristics :



The graph between output voltage and output current at constant input current is called as output characteristics. from the graph, it is seen that the curves are divided into 3 regions namely i) active region ii) cut-off region iii) saturation region.

i) active region -

In active region emitter junction is forward biased and collector junction is reverse biassed thus the transistor operates in normal mode. As collector voltage increases, the width of depletion layer increases this drcease the effective base width because of this the recombination's in the base region and hence, the base current decreases slightly this will increase the collector current. The dyamic output resistance is given by

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} \Big|_{I_B = \text{constant}}$$

ii) Cut-off-region -

The region below the curve $I_B = 0$ in fig is known as cut-off region. In this region both the junctions are reverse biased and only the leakage current flows through the transistor, the transistor is cut-off state and act as an open switch

iii) Saturation region -

In this region both the junctions are forward biased large current flows through the transistor & transistor acts as a close switch.

Q.2 Short answer question

i) Define α & β? Derive the relation between them

→ Current gain of transistor

In CB Configuration:

a) D.C Current gain :- The ratio of collector current to emitter current is called as dc current gain, denoted by α_{dc}

$$\alpha_{dc} = \frac{I_C}{I_E}$$

The value of α_{dc} is nearby equal to 1 but it is always less than 1 it never becomes greater then or equal to 1.

b) A.C current gain :- The ratio of change in collector current to change in emitter current at constant V_{CB} is called as ac current gain, denoted by α_{ac}.

$$\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E} \quad \Big| \quad V_{CB} = \text{constant}$$

The value of α_{ac} is nearly equal to 1

In CE Configuratin:

a) D.C current gain :- The ratio of collector current to base current is called as dc current gain, denoted by β_{DC}

$$\beta_{dc} = \frac{I_C}{I_B}$$

b) Ac current gain: The ratio of change in collector current to change in base current at constant V_{CE} is called as ac current gain, denoted by β_{ac}

$$\beta_{ac} = \frac{\Delta IC}{\Delta IE} \quad \Big| \quad V_{CE} = \text{constant.}$$

Relation between α_{dc} and β_{dc}

since $I_E = I_B + I_C$

Dividing both sides by I_C, we get

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

But $\frac{I_E}{I_C} = \frac{1}{\alpha_{dc}}$ and $\frac{I_B}{I_C} = \frac{1}{\beta_{dc}}$

i.e $\frac{1}{\alpha_{dc}} = \frac{1}{\beta_{dc}} + 1$

$\therefore \frac{1}{\alpha_{dc}} = \frac{1+\beta_{dc}}{\beta_{dc}}$

$$\alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}}$$

Simly,

$$\frac{1}{\alpha_{dc}} = \frac{1}{\beta_{dc}} + 1$$

$$\frac{1}{\beta_{dc}} = \frac{1}{\alpha_{dc}} - 1$$

$$\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$$

Relation between α_{ac} and β_{ac}

$$\alpha_{ac} = \frac{\beta_{ac}}{1+\beta_{ac}} \quad \& \quad \beta_{ac} = \frac{\alpha_{ac}}{1-\alpha_{ac}}$$

ii) Explain DC load line and Q-point

→ The DC load line is a graphical reprentation of the possible combinations of voltage and current that can be applied to a circuit element under DC conditions. It helps in analying the operating point of the circuit and determing the optical biasing conditions for the element.

The Q-point, also known as operating point or quiescent point, is the point on the DC load line where the element is biased to operate under normal opecating conditions. It represents

the voltage and current values that the circuit element will have when it is operating in a steady state with no input signal applied
Together, the DC load line and Q point are important in designing and analyzing electronic circuit because they determine the stability and performance of the circuit. The DC load line is used to find the Q point, and adjusting the biasing conditions of the circuit element can be used to move the Q point to achive the desribed performance characteristics

iii) Explain transistor leakage currents I_{CBO} and I_{CEO}

→ Transistar leakage currents are small current that flows theough a transistor when it is in an off-state, meaning there is no input signal applied. There are two types of transistor leakage currents :

1) collector-to-base leakage current (I_{CBO})
2) collector-to-emitter leakage current (I_{CEO})

1) I_{CBO} : It is the leakage current that flows from the collector to the base at a transistor when there is no input signal applied to the transistor. it occurs due to minarity comes that are genecated in the base region and diffuse into the collector region. I_{CBO} is typcally very small and is specified in the datasheet of the transistor, out it can increase with temperature and aging

2) I_{CBO} : It is the collector-emitter reverse bias leakage current, with flows when the base emitter junction is forwords-biased and the collector-emitter junction is reverse-biased, This current is also due to minority carriers, but it flows through the collector depetion region instead of the base region. I_{CEO} is typically larger than I_{CBO}, but it can also be minimized by paper transistor design and biasing

Overall, both I_{CBO} and I_{CEO} are important parameters to consider when desigaing trasistor circuits, as they can impact the overall performance and efficiency of the circuit.

DATE / /

Name :- Shreyash Dilip Awadi

Roll No :- 7201 Sub :- Electronic.

std :- BSC - I

14/20

Q1 Long answer questions [5mark]

i) Draw circuit arrangement to determine the input and output characteristics of CE configaration and explain them.

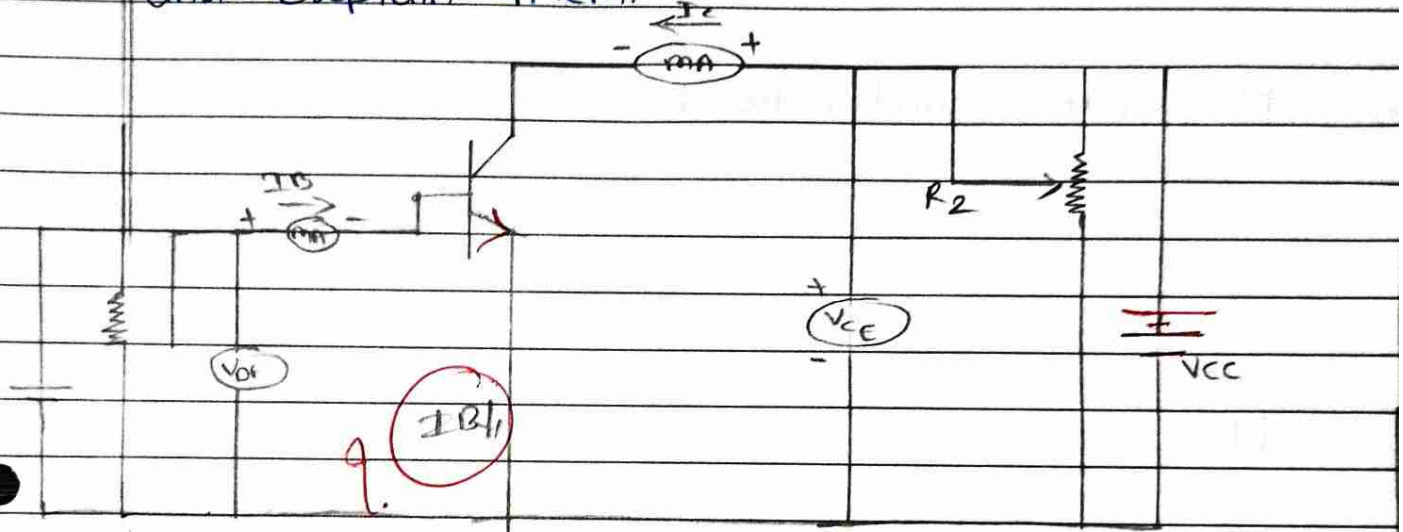
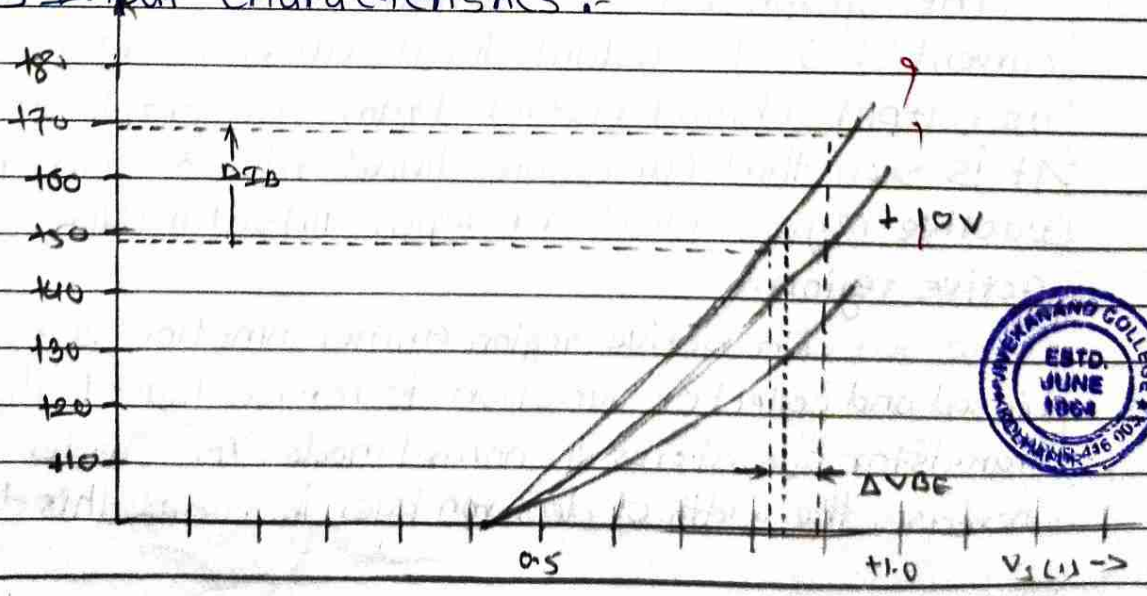


Fig 1.1

5 Fig 1i1 Shows the circuit arrangement for determining the characteristic of transistor in CE configration

a) Input characterisrics :-

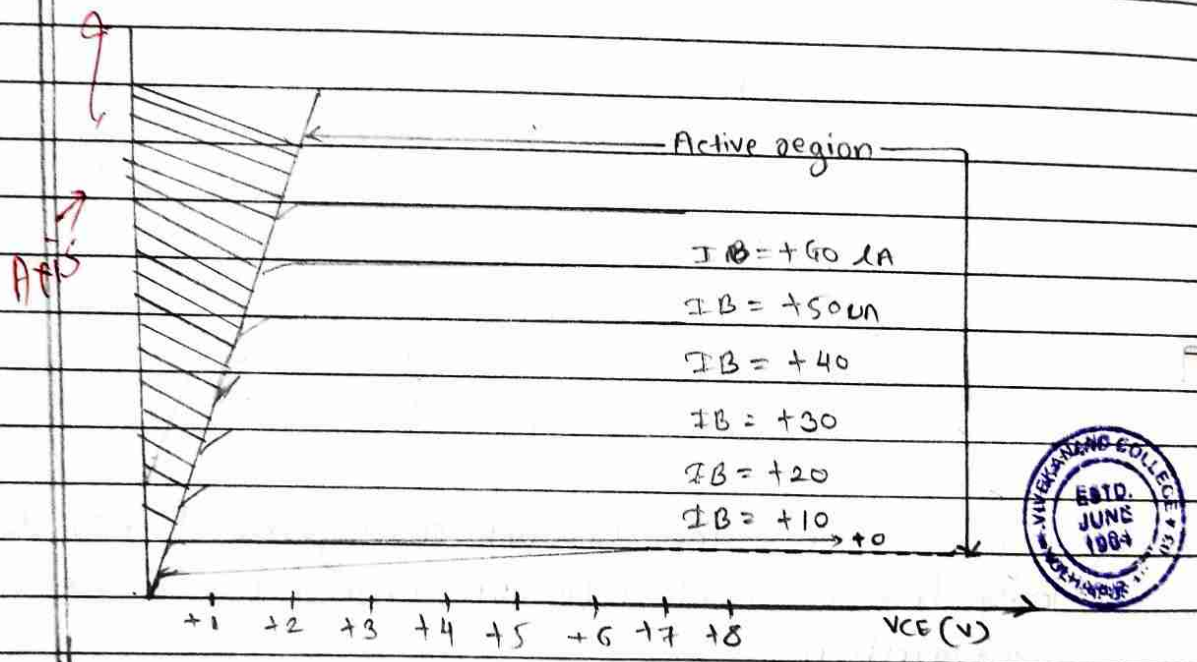


The graph ber^n input voltage (V_{BE}) and input current (I_B) at constant output voltage (V_{CE}) is called as input characteristics. From the circuit diagram in fig. 1.14, it is seen that the emitter base junction is forword biased. Hence current if increase exponentially will, in put voltage V_{BE} as shown in fig r is As collector voltage increases the curve shift rewards the right side this beause less base current flows for the same value of V_{CE}.

The dynamic input resistance is given by

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B} \Big|_{V_{CE} = \text{constant}}$$

b) output characteristics :-



The graph between output voltage (V_{CE}) and output current (I_C) at constant input current (I_B) is called as output charateristics fram the graph in fig 1.1b. It is seen that Curves are divided into 3 region namely i)active region ii)cut off region iii)saturation region

Active region.

In active region emitter junction is forword biased and collector junction is rererse biased thus the transistor operatores in normal mode. As covector voltage increase the width of depieron layer increases this decrease

the effective base width because of this recambinatio in the base region and hence, the base current decreases Slightly thes will increase the collector current. Thus, for given base current as collector voltage increases collector current also increase and the output are inclined as shown in graph in fig.

The dynamic output resistance is given by

$$r_o = \frac{\Delta V_{CB}}{\Delta I_C} \Big/ I_B = \text{constant}.$$

Cut - off region:-

The region below the curve $I_B = 0$ in fig 1.10 is known as cor. off region. In this region both the junctions are reverse blased and only the leakge current flows throug the transistar, the tragistor is in cut-off state and acts as an open switch.

Saturation regian:

In this region both the junctions are forword based large current flows through the transistore acts as a close switch.

Q2 Short answer questions:

1) Define α and β & Derive the reiation between them

→ a) DC current gain :- The ratio of collector (I_C) to emitter current (I_C) to emitter current (I_E) is called as dc current gain denated by α_{dc}.

$$\alpha_{dc} = \frac{I_C}{I_C}$$

b) A.C. current gain : The ratio of change in collentor current to change in emitter current at canstant V_{CB} is called as ac current gain denoted by α_{ac}

$$\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E} \Big/ V_{CB} = \text{contant}$$

DATE / /

Dc current :- The ratio of collector (I_C) is base current (I_B) called as dc current gain denoted by β_{dc}.

$$\beta_{dc} = \frac{I_C}{I_B}$$

A.c current :- The ratio of change in collector current to change in base current at constant V_{CE} is called ac current gain, denoted by β_{ac}.

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} \Big/ V_{CE} = \text{constant}.$$

4 Relation between α_{dc} and β_{dc}

since $I_E = I_B + I_C$

Dividing both sides by I_C, we get.

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

But $\frac{I_C}{I_E} = \alpha_{dc}$ and $\frac{I_B}{I_C} = \frac{1}{\beta_{dc}}$

i.e $\frac{1}{\alpha_{dc}} = \frac{1}{\beta_{dc}} + 1$

$$\frac{1}{\alpha_{dc}} = \frac{1 + \beta_{dc}}{\beta_{dc}}$$

$$\boxed{\alpha_{dc} = \frac{\beta_{dc}}{1 + \beta_{dc}}}$$

Simly, $\frac{1}{\alpha_{dc}} = \frac{1}{\beta_{dc}} + 1$

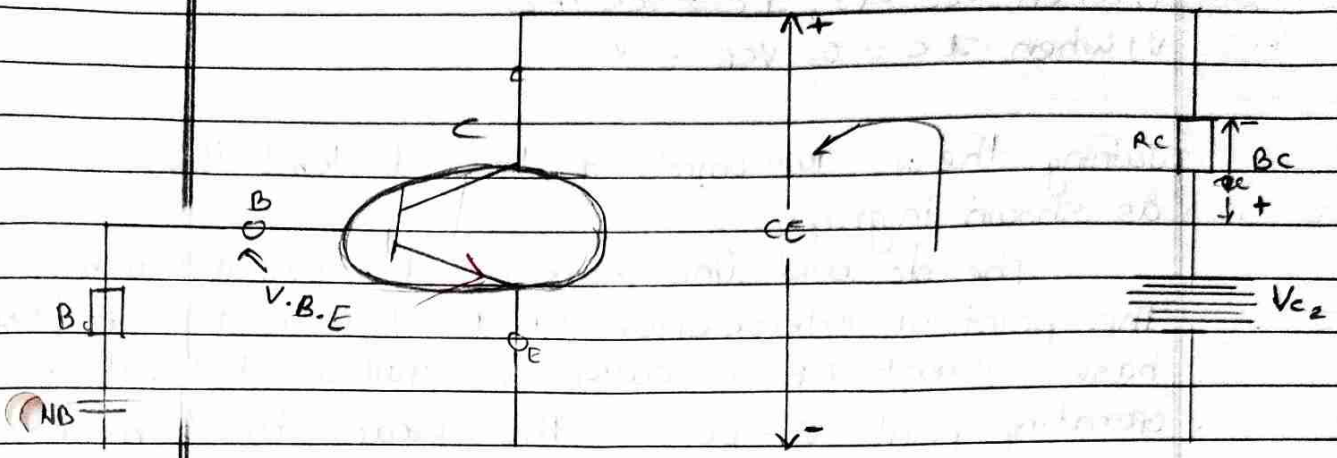
$$\frac{1}{\beta_{dc}} = \frac{1}{\alpha_{dc}} - 1 \qquad \boxed{\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}}$$

Relation between α_{ac} and β_{ac}

$$\alpha_{ac} = \frac{\beta_{ac}}{1 + \beta_{ac}} \quad \& \quad \beta_{ac} = \frac{\alpha_{ac}}{1 - \alpha_{ac}}$$

TEJ MY BRAIN
DATE / /

ii) Explain DC load line and Q-point



Consider a CE amplifier circuit without any a.c input signal. This condition is called qvipscent condition. The battery V_{cc} sends current I_c through the load resistance Rc & the transistor.

Applying kirchoff's voltage law to the collector circuit, we get —

$$V_{cc} = I_c R_c + V_{ce} \quad -- (1.8)$$

Rearranging and solving for I_c,

$$I_c = \left(-\frac{1}{R_c}\right) V_{ce} + \frac{V_{cc}}{R_c} \quad \ldots \text{G.T})$$

This eqn - is similar to $y = mx + c$ which is the equation of straight line. Thus platting eqn. (1.9) on the transistor output characteristic we get straight line whose slope $\left(-\frac{1}{R_c}\right)$ & intercept on the I_c axis is (V_{cc}/R_c). The slop of this line depends on the d.c load resistance Rc hence this line is called as d.c. load line.

3

From eq. (1.9) we have.

i) when $V_{CE} = 0$, $I_C = V_{CC}/R_C$

ii) when $I_C = 0$. $V_{CE} = V_{CC}$

Joining these two points a the dc load line as shown in graph.

The dc load line inersects the output curves. The point of intersection of load line for specified base current I_B is called as 'quipscent point or operating point 'Q-point'. The exact bcation of Q-point is decided by V_{CC}. R_C, R_B V_{BF} and V_{BB}. for given values of V_{CC} & R_C the Q. point depends upon the bace current I_B, which is calculate as follows.

Applying Kirchoff's vattage law to the base circuit we get

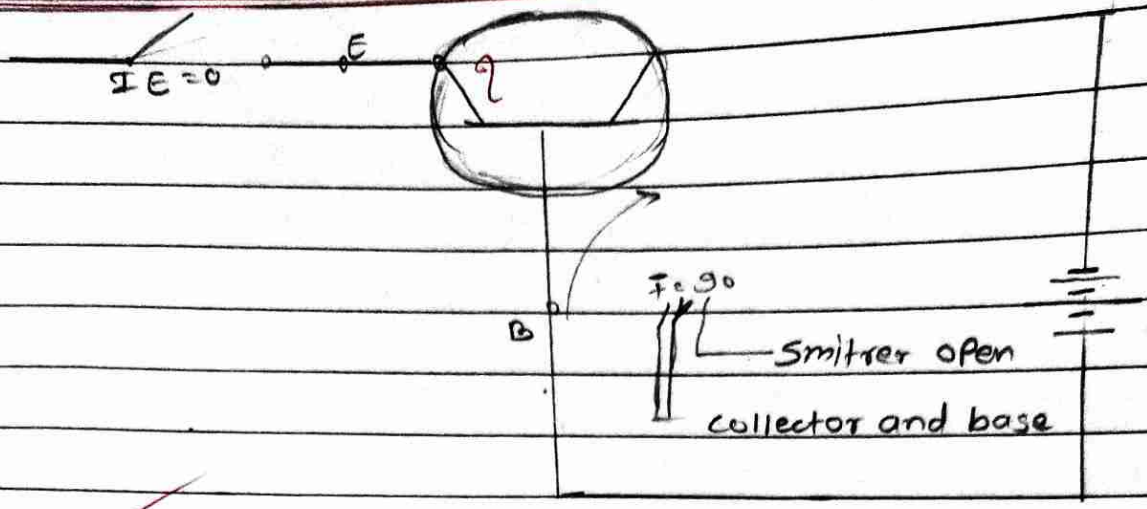
$$V_{BB} = I_B \cdot R_B + V_{BF}$$

$$I_B = \frac{V_{EB} - V_{EE}}{R_E} = \frac{V_{EF}}{R_E}$$

iii) Explain iransistor leakage current I_{CBO} & I_{CEO}

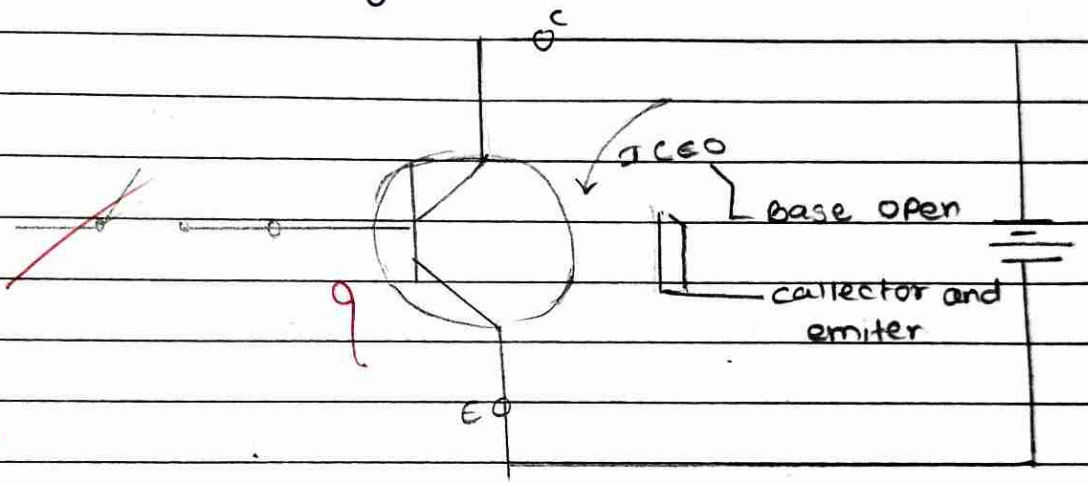
→ In CB- configuration – (I_{CBO})

If emitter ter minal is open ($I_E = 0$) then only reverse saturation current I_{CO} flows through the collector circuit This current is called as collector cut-off current, denoted by I_{CBO} or I_{CS} This current is very very small, because it is due to minority charge carrose. I_{CBO} increases. It dobles. It doubles for energy. 10°c rise in temperature.



Thus the total collector current is given by, $I_C = \alpha I_E + I_{CBO}$

In CE - configuration (I_C E 0)



Draw Neat Symbol

If base terminal is open ($I_B = 0$), then some leakage current flows through collector circuit. The current is called as collector cut-off current denoted by I_{CEO}.

Thus, the total collector current is given by $I_C = \beta I_B + I_{CEO}$.