"Dissemination of education through Knowledge, Science and culture
-Shikshanmaharshi Dr. Bapuji Salunkhe

**Shri Swami Vivekanand Shikshan Sanstha's**

# VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

Date: 11/04/2023

## Notice
## (B.Sc-I Electronics)

All the students of B.Sc-I Electronics are hereby informed that they should write a Home assignment on Unit II (Counters and shift registers) of (Digital Electronics-II) of total 20 marks on a full scape paper and submit to the department on or before 18/04/2023.

**Q.1 Long answer questions: [8 marks]**

i) Explain the decade asynchronous counter with logic diagram, truth-table and timing waveform.

**Q.2 Short answer questions: [4 *3=12 marks]**

ii) Explain working of 3 bit synchronous counter with logic diagram, truth-table and timing waveform.

i) Explain working of 4 bit left shift register with logic diagram.

iii) Explain working of ring counter with logic diagram.

(Dr. P. S. Jadhav)
Subject Teacher

Dr. C. B. Patil

HEAD
DEPARTMENT OF ELECTRONICS
VIVEKANAND COLLEGE, KOLHAPUR
(AUTONOMOUS)

VIVEKANAND COLLEGE ESTD. JUNE 1964 KOLHAPUR 416 003

Shri Swami vivekanand Shikshan Santha's

# VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

## B.Sc . - I 2022-23

## Digital Electronics

## Assignment II :Unit -II Counters and shift Registors

| Sr. No. | Roll No. | Student Name | Assignment Submitted | Marks |
|---|---|---|---|---|
| 1 | 7201 | AWATI SHREYASH DILIP | Submitted | 19 |
| 2 | 7204 | KAMBLE SAURABH SANJAY | not submitted | 0 |
| 3 | 7207 | LOKHANDE SUJAL SANDIP | not submitted | 0 |
| 4 | 7208 | MANGAONKAR VEDANT PRASHANT | Submitted | 20 |
| 5 | 7209 | MISAL OMKAR SUNIL | Submitted | 18 |
| 6 | 7210 | MUJAWAR ZAHIR JAMIR | not submitted | 0 |
| 7 | 7211 | NESARKAR SIDDHARTH DEEPAK | Submitted | 19 |
| 8 | 7214 | PATIL HARSHAD RAJGONDA | Submitted | 19 |
| 9 | 7215 | PATIL HARSHVARDHAN DHANANJAY | Submitted | 19 |
| 10 | 7223 | WARANGE NIRAJ RAJESH | Submitted | 20 |
| 11 | 7224 | YADAV HARSH NIVAS | not submitted | 0 |
| 12 | 7229 | BHADARAGE ABHISHEK SUNIL | Submitted | 19 |
| 13 | 7279 | ALANBAGI AHMED QASIM HASAN | Submitted | 17 |
| 14 | 7281 | ASANEKAR YASH TUKARAM | Submitted | 20 |
| 15 | 7282 | BAMANE SAHIL NIVRUTI | Submitted | 18 |
| 16 | 7283 | BAVACHE SHRAVANI BHIMRAV | Submitted | 19 |
| 17 | 7284 | CHOUGULE SAI CHANDRAKANT | Submitted | 18 |
| 18 | 7285 | CHOUGULE VAIBHAVI JAYSING | Submitted | 18 |
| 19 | 7286 | DHUMALE SANIKA SANTOSH | Submitted | 19 |
| 20 | 7287 | GHUMAI DHIRAJ BABASO | not submitted | 0 |
| 21 | 7288 | GURAV SANIKA RAVINDRA | Submitted | 20 |
| 22 | 7289 | HIRDEKAR SHREYA SHASHIKANT | Submitted | 20 |
| 23 | 7291 | KANGRALKAR GAYATRI GUNDU | Submitted | 19 |
| 24 | 7292 | KUMBHAR DIKSHA YUVRAJ | Submitted | 19 |
| 25 | 7293 | KUMBHAR PRATHMESH YUVRAJ | Submitted | 17 |
| 26 | 7294 | KUMBHAR SANIKA SANJAY | Submitted | 20 |
| 27 | 7296 | MANE AARATI PRAKASH | Submitted | 20 |
| 28 | 7297 | MANE ADITYA SHARAD | Submitted | 15 |
| 29 | 7299 | NANAVARE ADARSH VIJAY | not submitted | 0 |
| 30 | 7301 | NIMBALKAR SAIRAJ NANDKUMAR | Submitted | 18 |
| 31 | 7302 | PARPOLKAR SANIKA SUBHASH | Submitted | 20 |
| 32 | 7303 | PATIL ADITYA MANSING | Submitted | 0 |
| 33 | 7304 | PATIL KIRTI SAMBHAJI | Submitted | 20 |
| 34 | 7305 | PATIL POONAM NARSU | Submitted | 20 |
| 35 | 7306 | PATIL PRADNYA PRADIP | Submitted | 18 |
| 36 | 7307 | PATIL PRATHAMESH BHAGAVAN | Submitted | 18 |
| 37 | 7308 | PATIL RAVIRAJ BAJIRAO | not submitted | 0 |

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| | | | | |
|---|---|---|---|---|
| 38 | 7309 | PATIL RIYA NITIN | Submitted | 17 |
| 39 | 7310 | PATIL SAHIL VISHNU | Submitted | 12 |
| 40 | 7311 | PATIL SAMARTH SHRIKANT | Submitted | 18 |
| 41 | 7312 | PATIL SAMMED DHANYAKUMAR | not submitted | 0 |
| 42 | 7313 | PATIL SOURABH BHAGAWAN | Submitted | 19 |
| 43 | 7314 | PHADAKE SUMIT RAMBHAU | not submitted | 0 |
| 44 | 7317 | SAWANT PRATHAM PRADEEP | Submitted | 19 |
| 45 | 7318 | SHETE ANUSHKA SUNIL | Submitted | 20 |
| 46 | 7319 | SURVE VIKRANT RAJENDRA | Submitted | 17 |
| 47 | 7320 | TIWADE KETAN GIRISHKUMAR | Submitted | 19 |
| 48 | 7325 | GHODE VAISHNAVI SHRIKANT | Submitted | 17 |
| 49 | 7332 | LAMBE SANKET JAYKUMAR | Submitted | 20 |
| 50 | 7333 | LOLAGE GAYATRI GAJANAN | Submitted | 18 |
| 51 | 7344 | PATIL SHARVARI KULDEEP | Submitted | 19 |
| 52 | 7550 | DADDIKAR GAURAV NITIN | not submitted | 0 |
| 53 | 7551 | ALTEKAR ADITYA MAHESH | Submitted | 20 |
| 54 | 7563 | AHMED SAMI ALITTIBIN | Submitted | 17 |
| 55 | 7567 | PATIL SWAPNIL SURESH | Submitted | 20 |
| 56 | 7569 | SHINDE RUGVED TANAJI | not submitted | 0 |
| 57 | 7584 | PATIL PRATHMESH KALLAPPA | Submitted | 19 |

Subject Teacher
Dr.P.S.Jadhav

Head of the Department
Dr. C.B.Patil

VIVEKANAND COLLEGE ESTD. JUNE 1964 KOLHAPUR-416 003

HEAD
DEPARTMENT OF ELECTRONICS
VIVEKANAND COLLEGE, KOLHAPUR
(AUTONOMOUS)

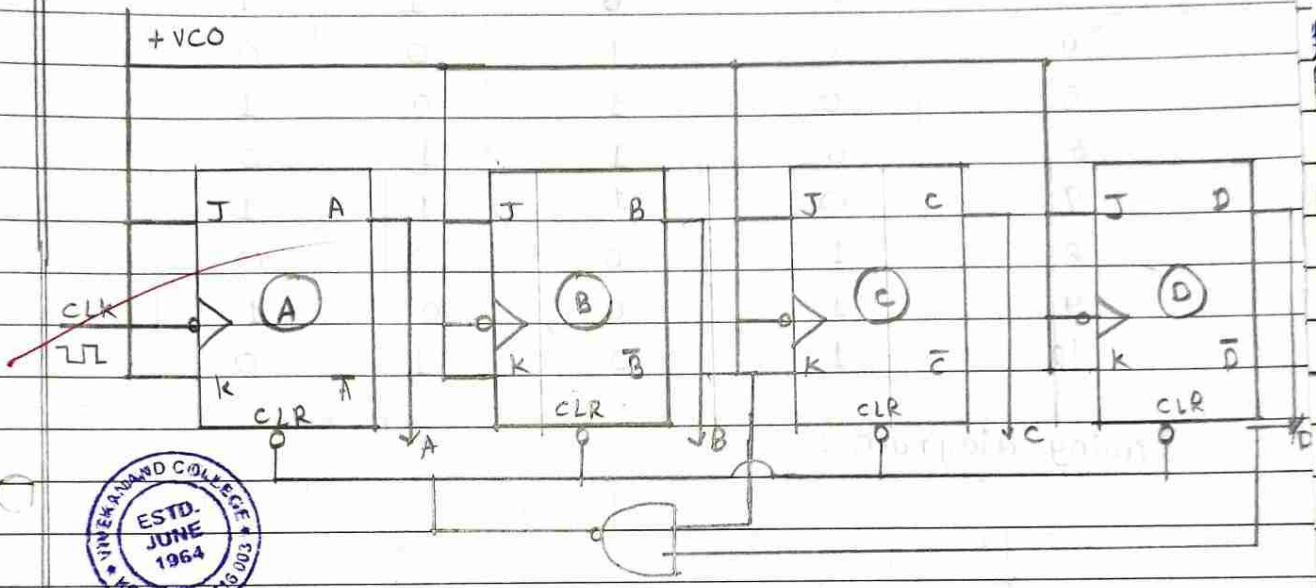
Name - Vaishnavi Ghode
Roll no - 7325

17/20

GoodLuck | Page No.
Date

Q.1 Explain the decode asynchronous counter with logic diagram, truth-table and timing waveform

→ A decade (mod-10) counter has modified count by using 4 negative-edge triggred J-K flip-flop modified is counter can be construted. 6 (x states are not used (from 1010 to 1111). The counter must reset at the end of 10th CLK pulse. feedback is used for skipping unwanted states.



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Decade counter consists of four negative edge triggered flip-flop. J&K inputs of all flip-flops are connected to the +ve (logic). clock drives flip-flop output of flip-flop A drivers fip-flop B. output of flip-flop B drives flip-flop C. output of flip-flop c drives flip-flop D on the negative edge of the 10th clock pulse. A changes from 1 to 10 therefore B changes 0 to 1. This being a positive change. flip-flop C & D are not affected.
∴ DCBA = 1010 but this state is mamentary state. to all the NAND gate provides a Reset (clear) pluse to all flip-flop as B = 1, D = 1 Because B & D are applied to NAND gate. Therefore Counter is reset

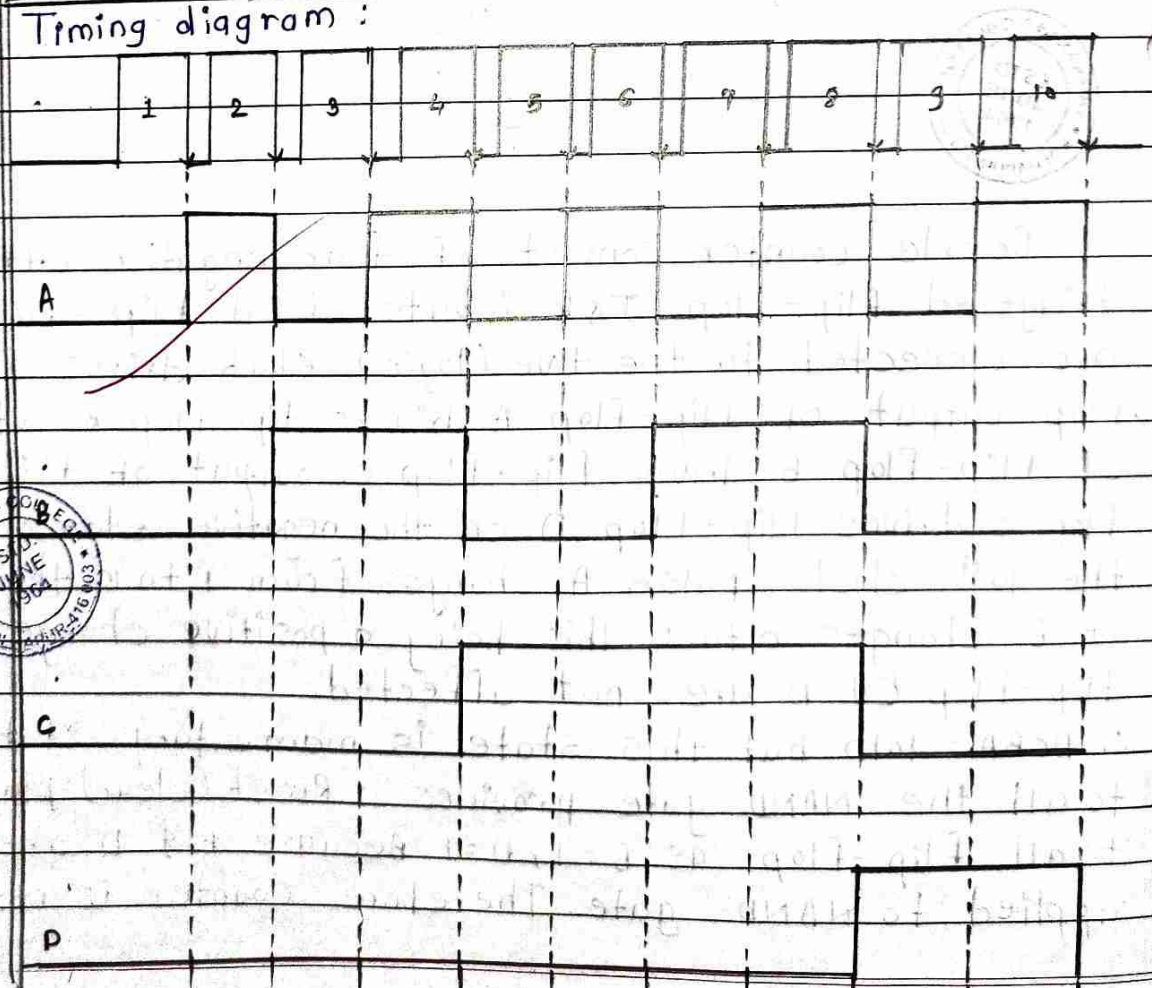
Goodluck

States in 16 states are skipped & it works as decade Counter

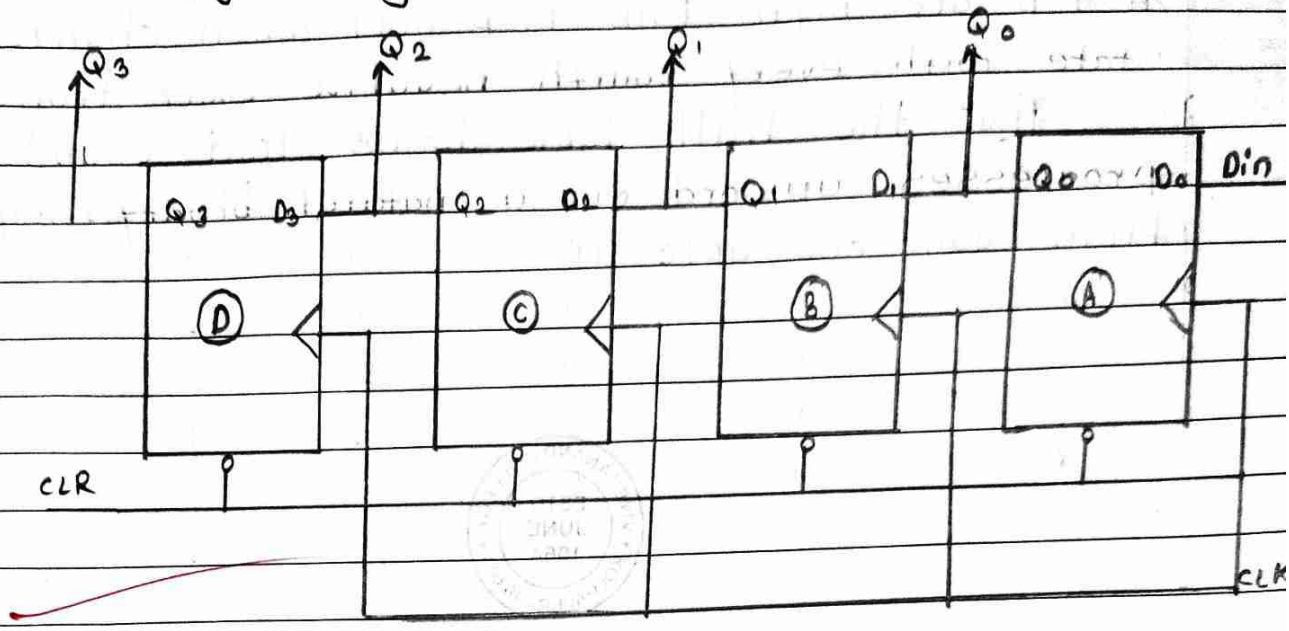
Truth Table :

| Clk Pulse | D | C | B | A |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |

Timing diagram :



Q.2 i] Explain working of 4 bit left shift register with logic diagram.



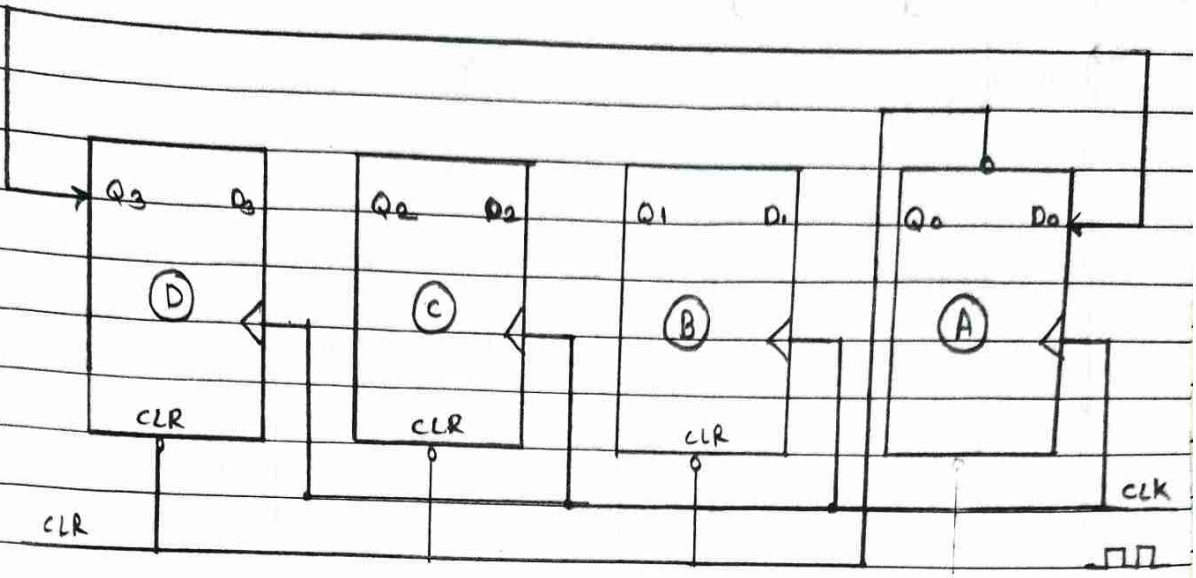

left shif Register.

Since AND gate is enabled and will transmit the clock to the flip-flop C only when both A & B are high flip-flop only when changes state with every fourth negative clock transition

Thus the truth-table shows that counter progresses upword sin a natural binary sequence from count 000 upto 111

Date

ii] Explain working of ring counter with logic diagram




Ring Counter can be constructed using D filp-flops. Any external data input is not applied $Q_0$ is Connected to $D_1$, $Q_1$ to $Q_2$, $D_2$ to $D_3$. $Q_3$ to $D_0$, $Q_0$ is Initially a low pulse is applied to PR input of first flip-flop. Therefore stored word becomes,

$$Q = Q_3\ Q_2\ Q_1\ Q_0 = 0001$$

On the positive edge of the first clock pulse (Q)= 0010 on the positive edge of the second clock pulse (Q) = 0100 on the positive edge of the third clock pulse (Q) = 1000 on the positive edge of the fourth clock pulse (Q) = 0001

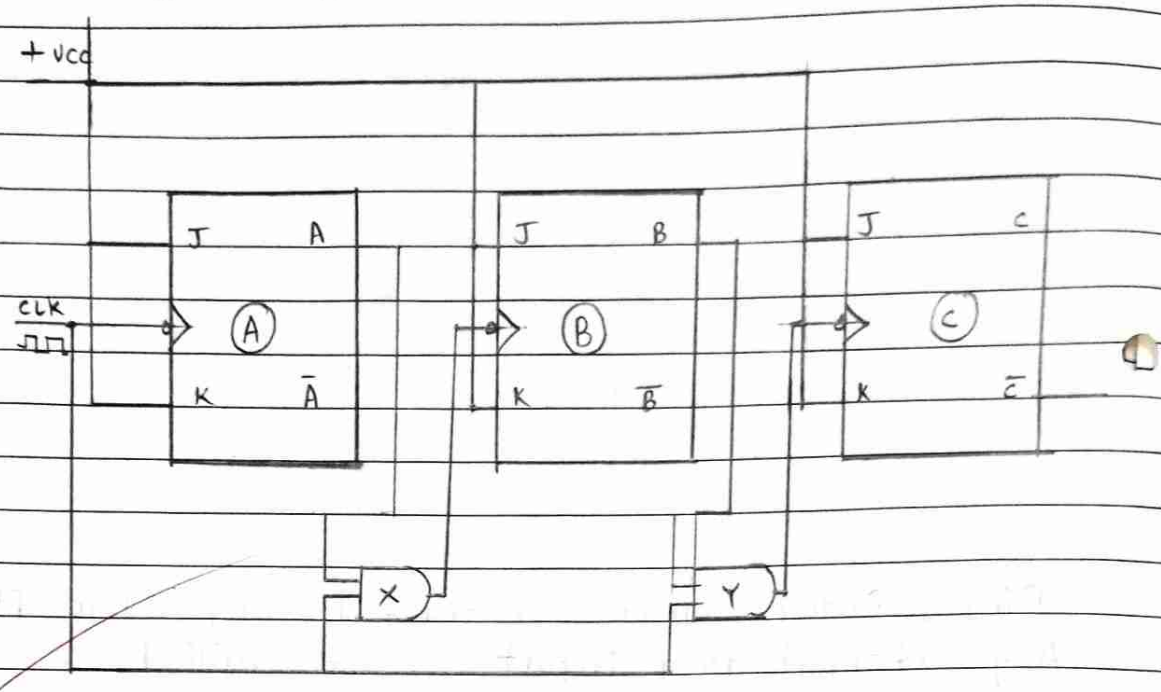
Thus cycle is complete. The stored bit follows a circular path moving left through the flip-flops untill the final flip-flop sent it back to the first flip-flop. This action is similar to left shift register but in this $Q_3$ is given to $D_0$ as cycle occurs this counter is called as ring counter



Goodluck

iii] Explain working of 3 bits synchromus Counter with logic diagram, truth table and timing waveform.

→




Truth table :

| CLK | C | B | A |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |
| 8 | 0 | 0 | 0 |



In mod-8 Counter 3 J.K flip-flops are used. J & K are connected to +vcc. Each flip-flop will toggle with negative clock transition at its clock input.

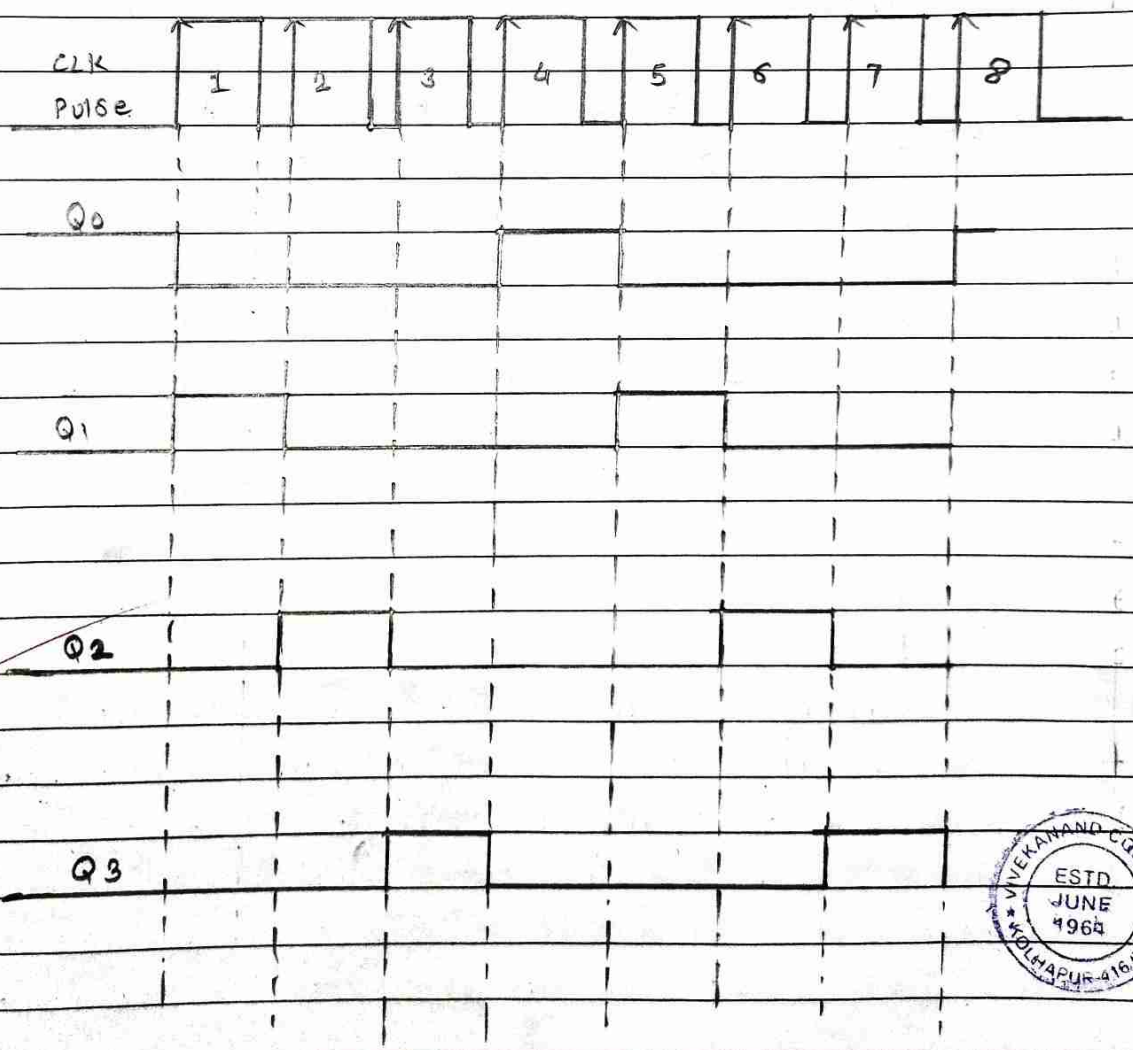
Flip-flop a changes states with each negative clock transition. whenever A is high 'x' gate is enabled & clock pulse is passed through the gate to the clock input

of flip-flop B. Thus B changes state with every second negative transition.

Truth table:

| CLK Pluse | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 1 | 0 | 0 | 0 |
| 4 | 0 | 0 | 0 | 1 |
| 5 | 0 | 0 | 1 | 0 |
| 6 | 0 | 1 | 0 | 0 |
| 7 | 1 | 0 | 0 | 0 |
| 8 | 0 | 0 | 0 | 1 |

Waveform:



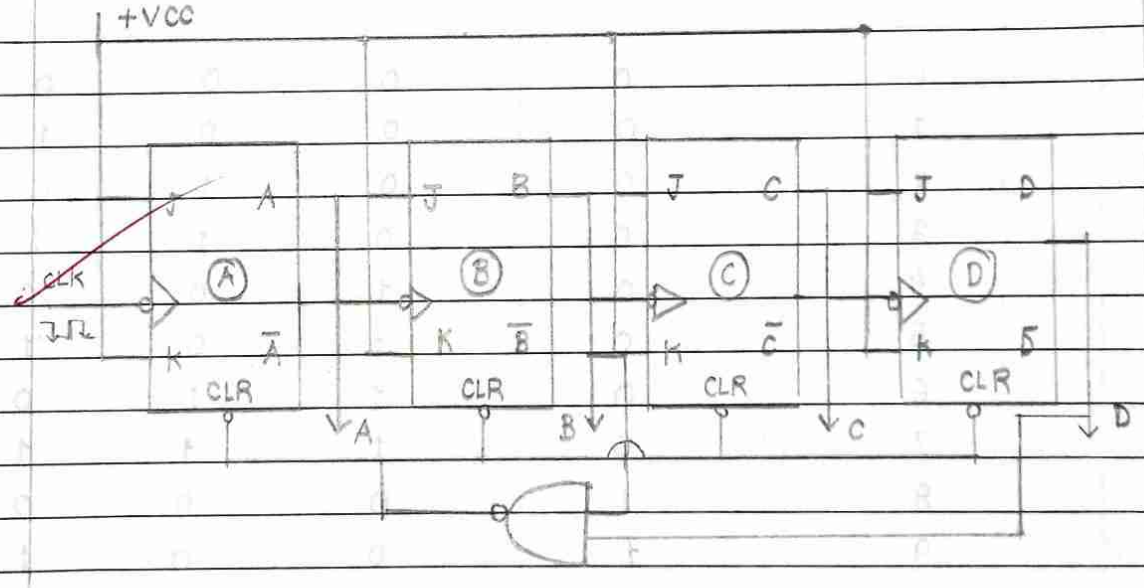
20/20 Page No.: Date:

Anushka Sunil Shete
Roll No: 7318
Class : BSC-FY

# Assignment

Q1. i] Explain the decade asynchronous counter with logic diagram, truth-table and timing waveform.

→ A decade (mod-10) counter has modified count by using 4 negative-edge triggered J-K flip-flop. modified 16 counter can be constructed. six states are not used (from 1010 to 1111). The counter must reset at the end of 10th CLK pulse. feedback is used for skipping unwanted states.




Decade counter consists of four negative edge triggered Flip-Flop. J & K inputs of all flip-flops are connected to the +Vcc (logic 1). Clock drives Flip-Flop A output of flip-flop A drives flip-flop B. output of Flip-flop B drives flip-flop C. output of flip-flop C drives flip-flop D.

on the negative edge of the 10th clock pulse. A changes from 1 to 10 therefore B changes 0 to 1. This being a positive change. Flip-Flops C & D are not affected.

∴ DCBA = 1010 but this state is momentary state.

The NAND gate provides a Reset (clear) pulse to all flip-flops as B=1, D=1. Because B & D are applied to NAND gate. Therefore counter is reset & states in 16 states are skipped & it works as decade counter.

Truth Table:

| CLK Pulse | D | C | B | A |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |

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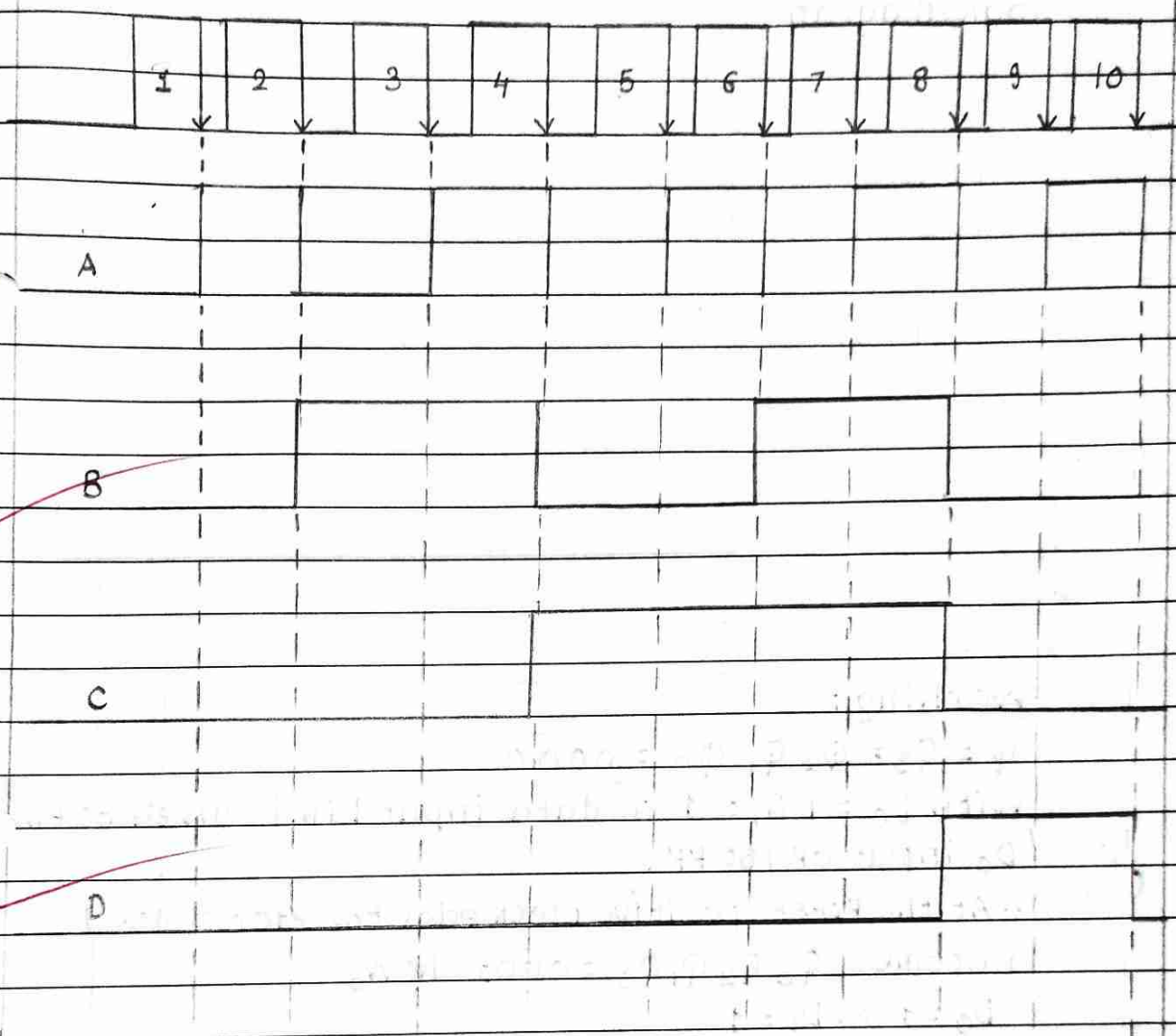
## Timing diagram:



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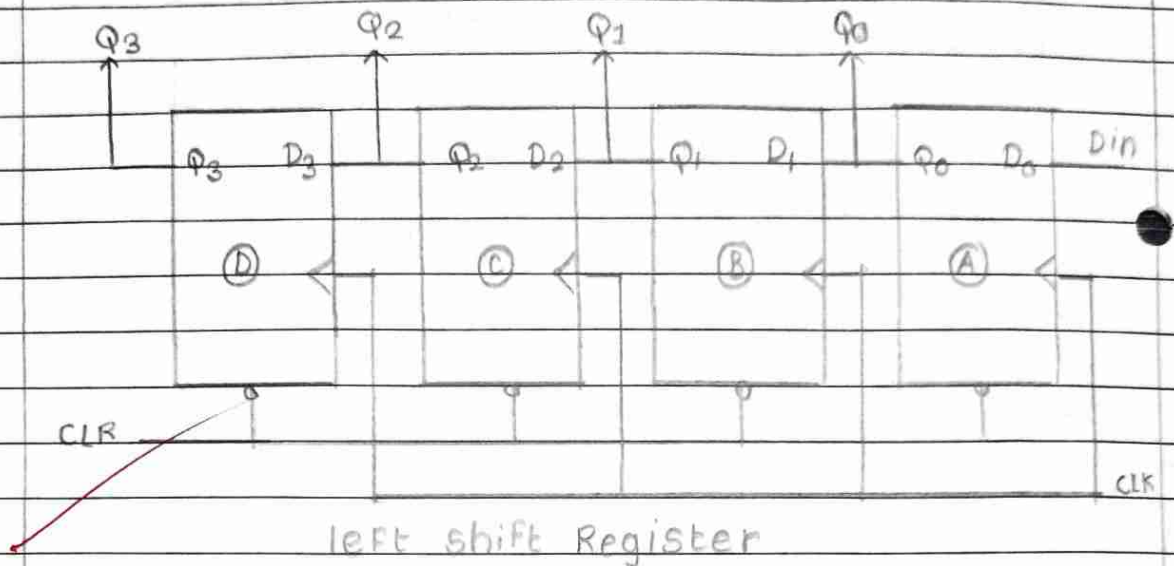
Q2.

i] Explain working of 4 bit left shift register with logic diagram.




left shift Register

working:

$Q = Q_3 Q_2 Q_1 Q_0 = 0000$

with $D_0 = Din = 1$ i.e data input Din is given to the $D_0$ input of 1st FF.

∴ At the first positive clock edge the stored code becomes $Q_3 Q_2 Q_1 Q_0 = 0001$ Now,

$D_0 = 1$ & $D_1 = 1$

on the second positive clock edge output Q = 0011

on the third positive clock edge output Q = 0111

on the Fourth positive clock edge output Q = 1111

As long as Din = 1, the stored code (data) remains unchanged. Now IF Din is changed to zero. Then at each successive clock pulse provides Following output.

i.e

| $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|
| 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 |

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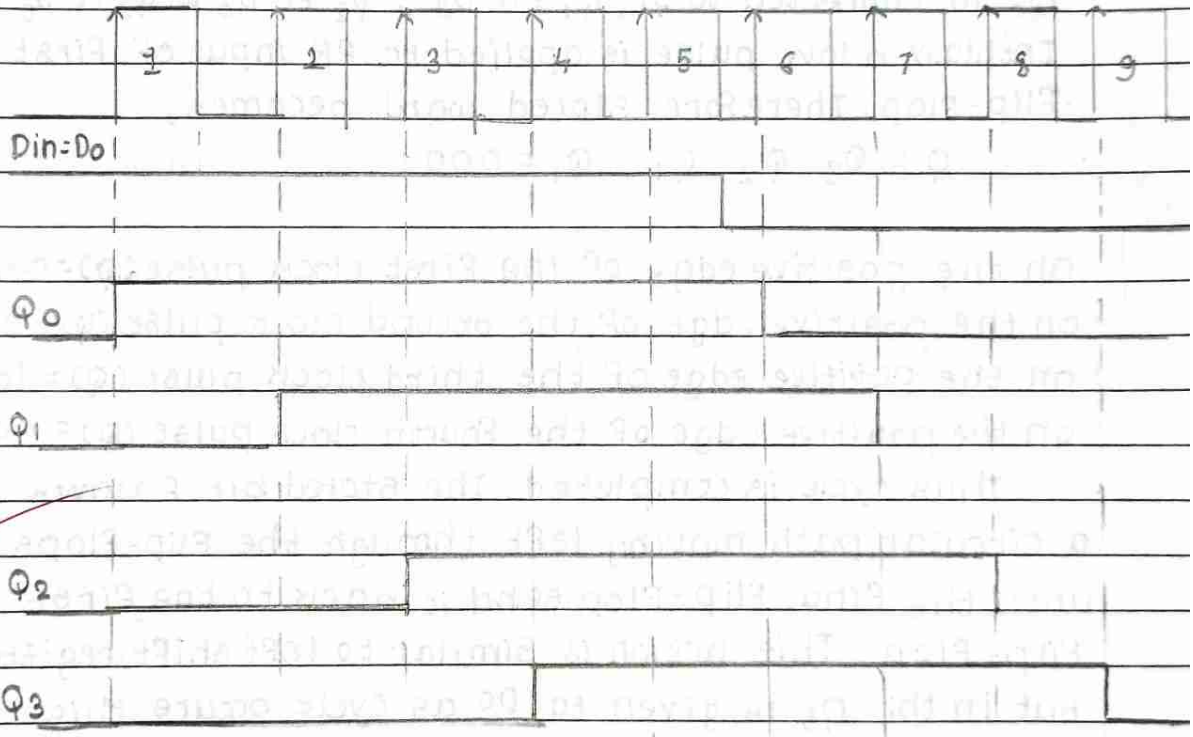
since AND gate is enabled and will transmit the clock to the Flip-Flop C only when both A & B are high Flip-Flop C only when changes state with every Fourth negative clock transition.

Thus the truth-table shows that counter progresses upwards in a natural binary sequence from count 000 upto 111.

As long as Din=0, subsequent clock pulses have no effect.

Timing diagram:



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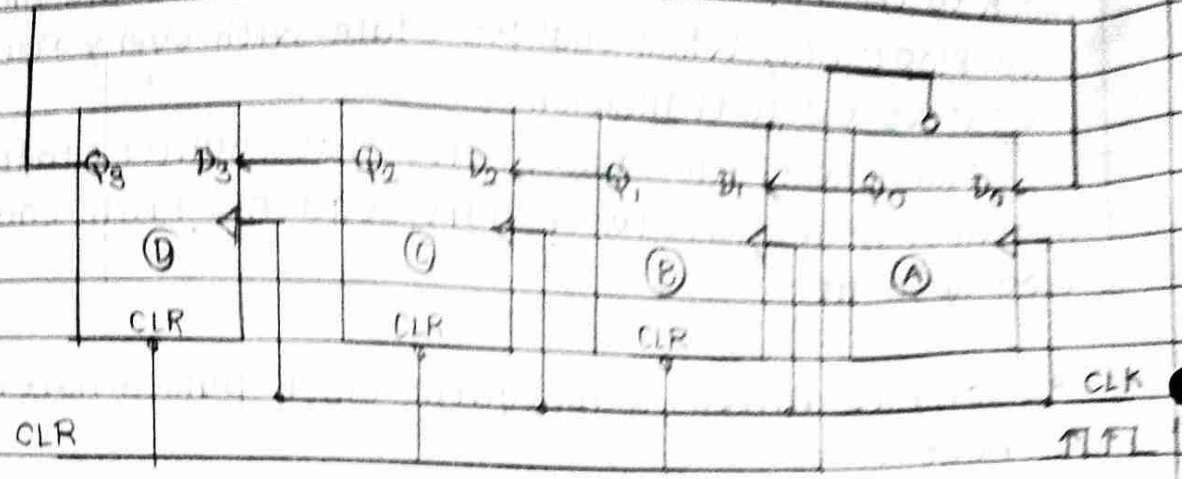
iii] Explain working of ring counter with logic diagram.




Ring counter can be constructed using D flip-flops.
Any external data input is not applied.
$Q_0$ is connected to $D_1$, $Q_1$ to $D_2$, $Q_2$ to $D_3$ & $Q_3$ to $D_0$
Initially a low pulse is applied to PR input of first Flip-Flop. Therefore stored word becomes,

$$Q = Q_3\ Q_2\ Q_1\ Q_1 = 0001$$

On the positive edge of the first clock pulse (Q) = 0010
on the positive edge of the second clock pulse (Q) = 0100
on the positive edge of the third clock pulse (Q) = 1000
on the positive edge of the fourth clock pulse (Q) = 0001

Thus cycle is completed. The stored bit follows a circular path moving left through the Flip-flops. until the final flip-flop send it back to the first Flip-flop. This action is similar to left shift register but in this $Q_3$ is given to D0 as cycle occure this counter is called as ring counter.

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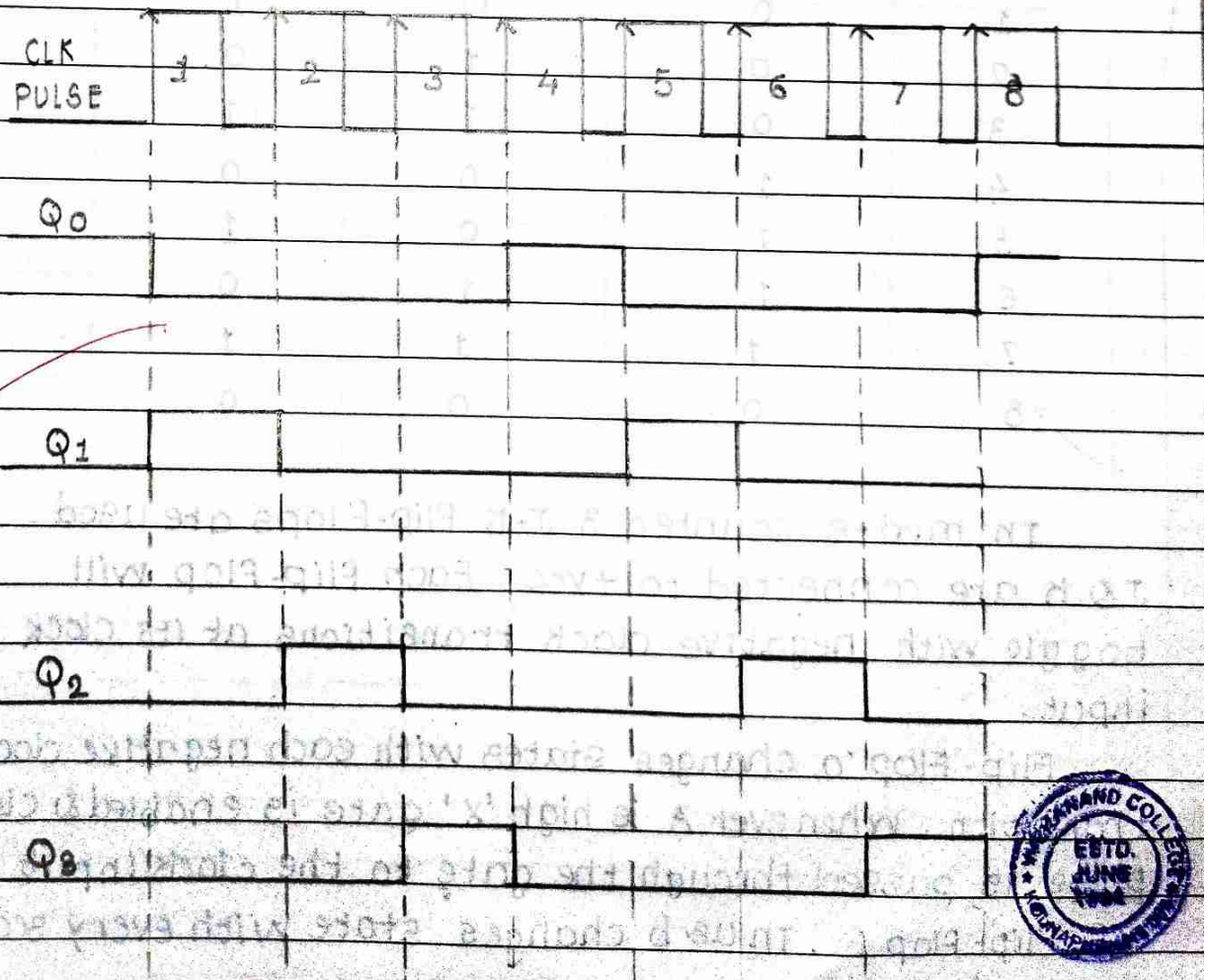
Truth table:

| CLK Pulse | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 2 | 0 | 1 | 0 | 0 |
| 3 | 1 | 0 | 0 | 0 |
| 4 | 0 | 0 | 0 | 1 |
| 5 | 0 | 0 | 1 | 0 |
| 6 | 0 | 1 | 0 | 0 |
| 7 | 1 | 0 | 0 | 0 |
| 8 | 0 | 0 | 0 | 1 |

Waveform :-



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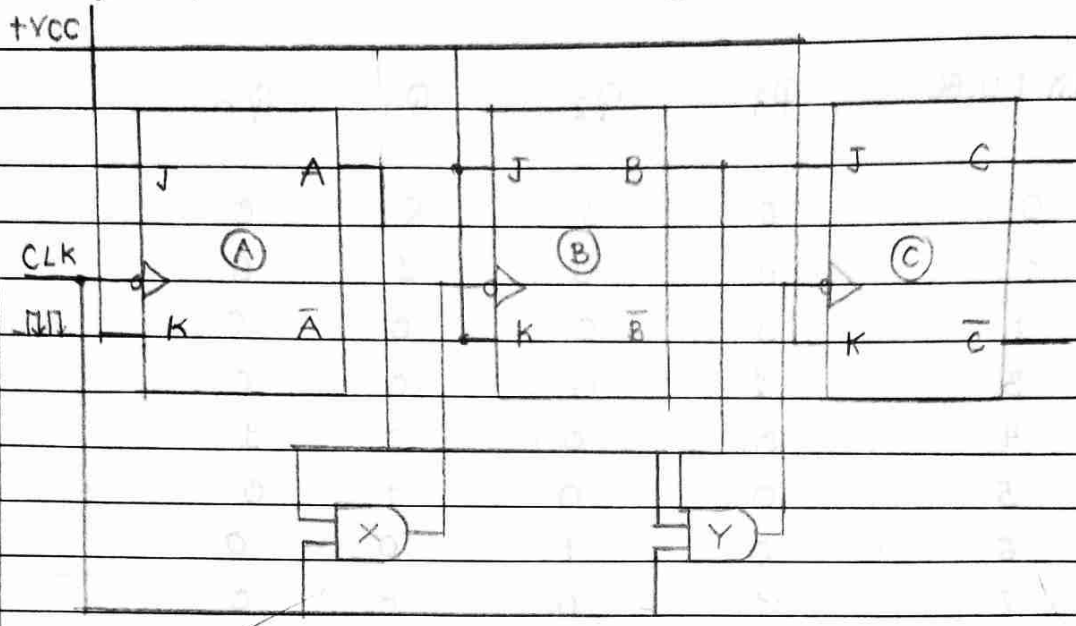
iii) Explain working of 3 bit synchronous counter with logic diagram, truth table and timing waveform.




Truth table:

| CLK | C | B | A |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |
| 8 | 0 | 0 | 0 |

In mod-8 counter 3 J-K Flip-Flops are used. J & K are connected to +Vcc. Each Flip-Flop will toggle with negative clock transitions at its clock input.

Flip-Flop 'a' changes states with each negative clock transition. whenever A is high 'x' gate is enabled & clock pulse is passed through the gate to the clock input of Flip-Flop B. Thus B changes state with every second negative transition.

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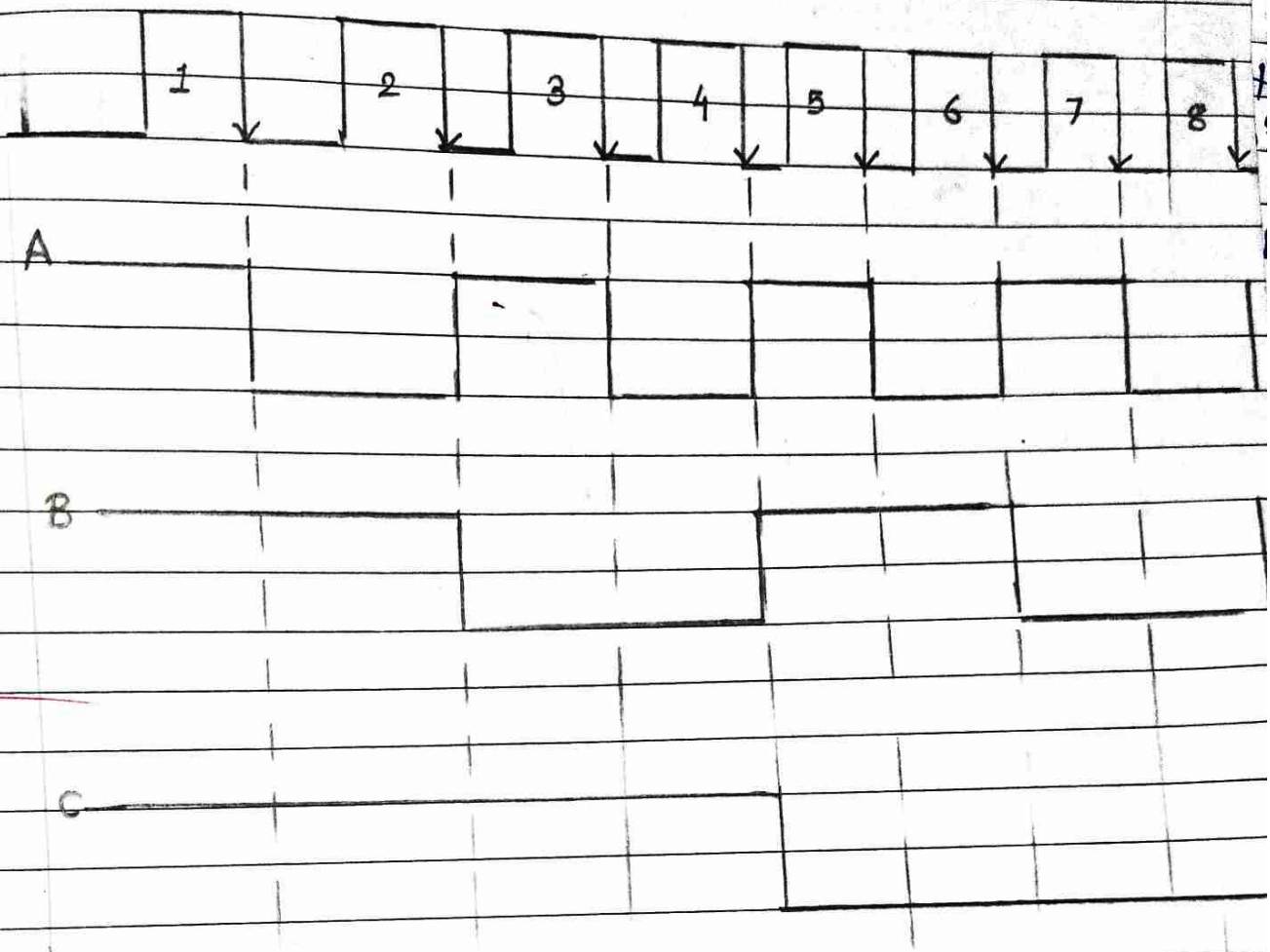
# Timing waveform:



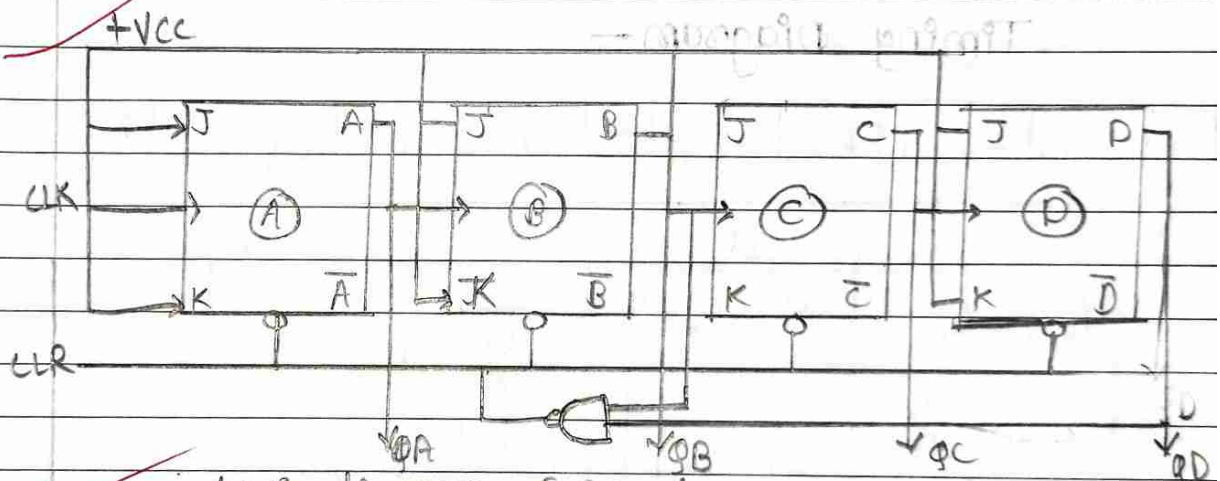
18/20

Name - Prathamesh Bhagavan Patil
Roll No - 7307
Std - BSc - FY  DIV - A

Q.1 Long answers questions.

1) Explain the decade asynchronous counter with logic diagram, truth-table and timing. Waveform.

→ A decade counter has modified count. By using 4 negative edge triggered J-K flip-flop modified 16 counter can be constructed. It has 16 states but decade counter has 10 states six states are not used. the counter must reset at the end of 10th CLK pulse feedback is used for skipping unwanted states.




Logic diagram of Decade counter

Decade counter consist of four negative edge triggered ff are cascaded J and K inputs of all flip-flops connected to the +ve clock drives FF H. O/P of FF A derives FFB O/P of FFB derives FFC of FFC derives FFD.

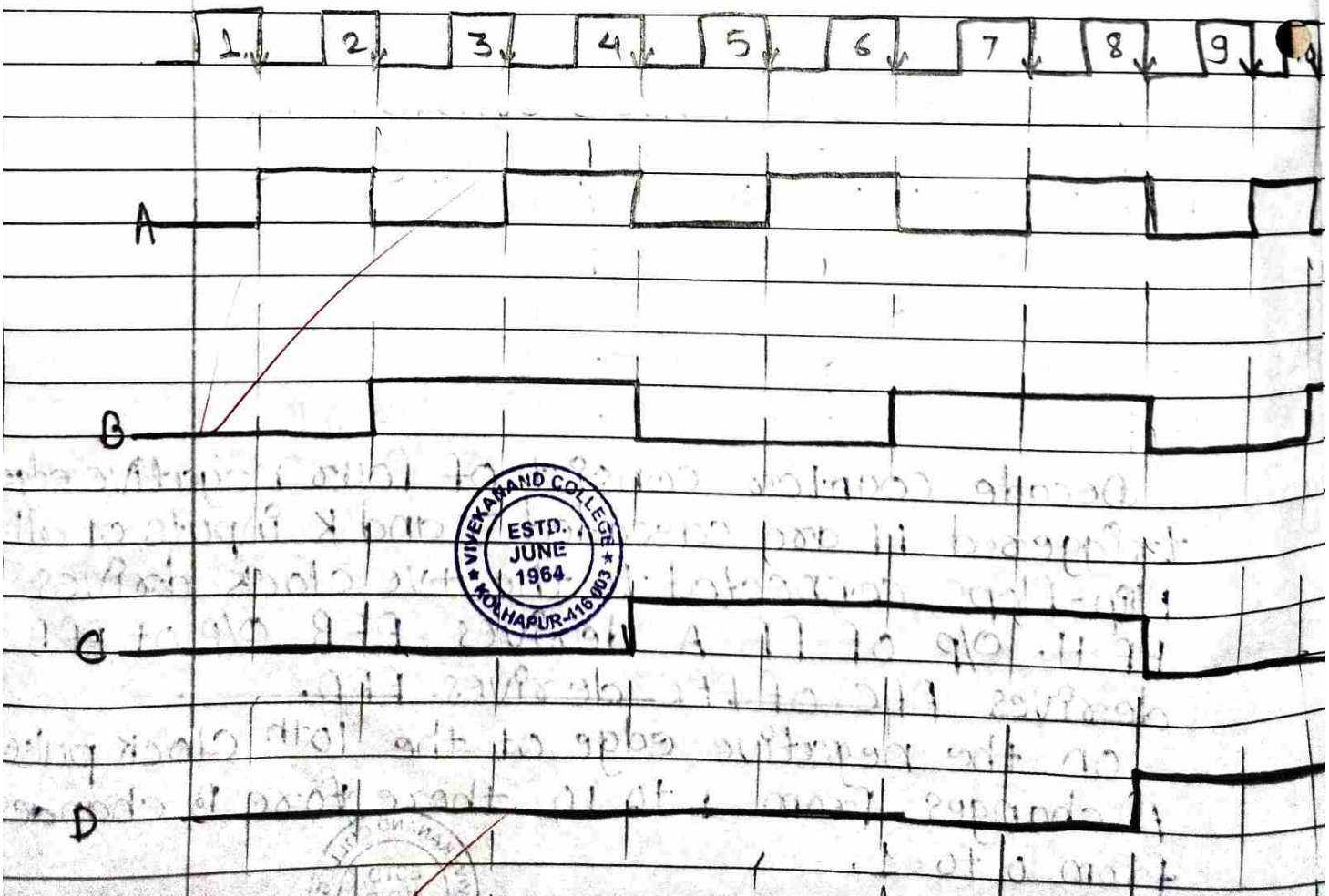
on the negative edge of the 10th clock pulse. A changes from 1 to 10 therefore B changes from 0 to 1.

This being a positive change flip-flops C and D are not affected ∴ DCBA = 1010 but this state is momentary state.

Truth-table -

| CLK Pulse | D | C | B | A |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |

Timing Diagram —



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Q.2. Short answer questions.

1) Explain working of 3 bit synchronous counter with logic diagram, truth-table & timing waveform.

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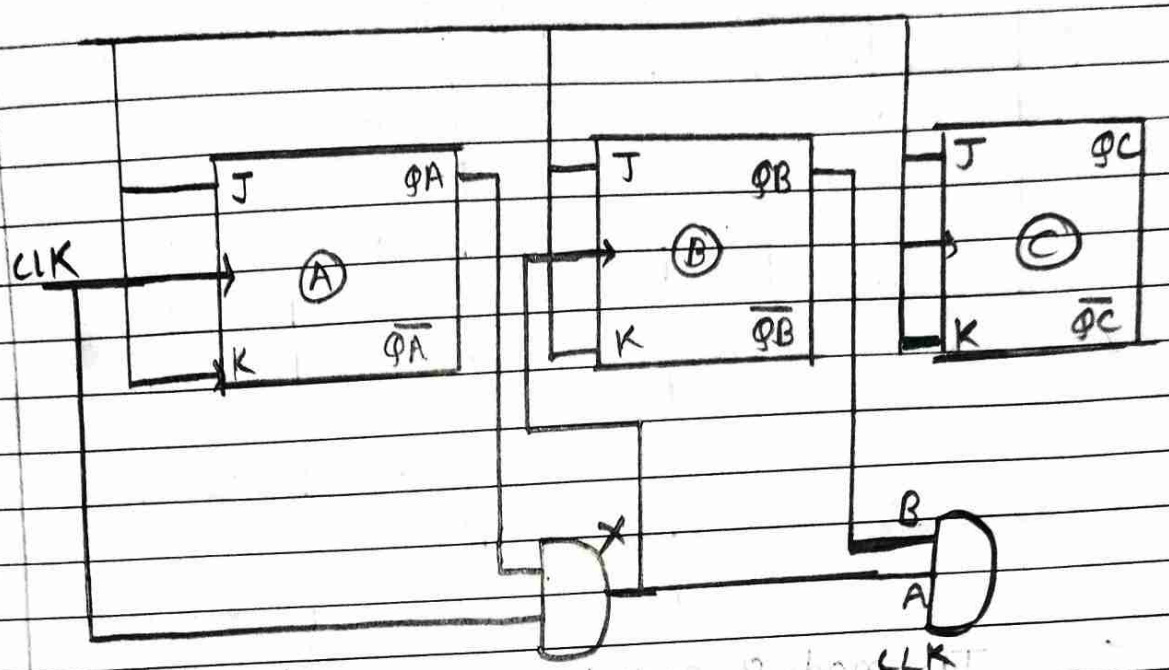
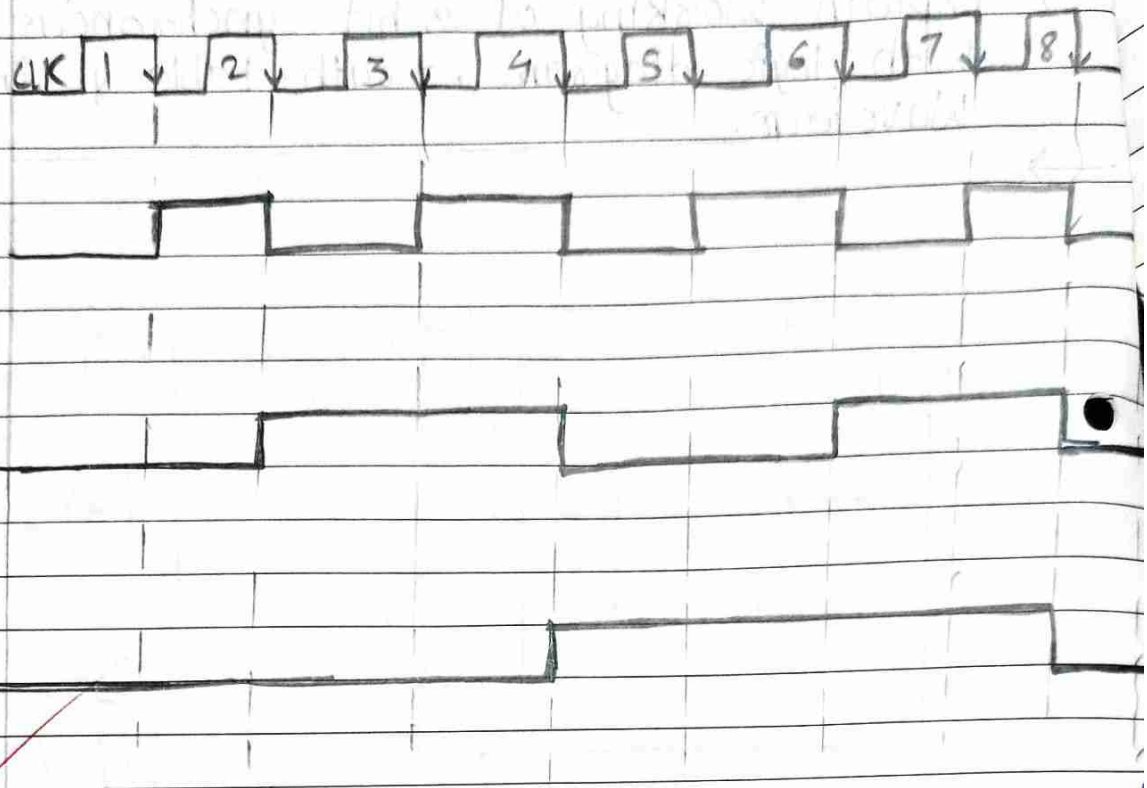



Logic diagram

Truth - Table

| CLK Pulse | C | B | A |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |
| 8 | 0 | 0 | 0 |

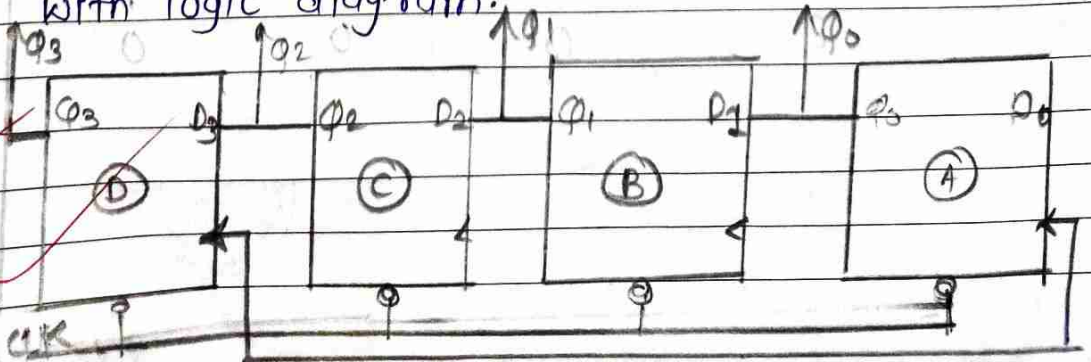
Timing diagram-




In mod-8 counter 3 J-K flip-flops are used J & K inputs are connected to +Vcc Each flip-flop will toggle with negative clock transitions at its clock. input flip-flop A changes state with each negative clock transition whenever A is high 'X' gat is enabled. and clock pulse is passed through the gate to the clock input of flip-flop B. Thus B changes state with every second negative transition.

Thus the truth-table shows that counter progresses upwards in a natural binary sequence from count 000 upto 111.

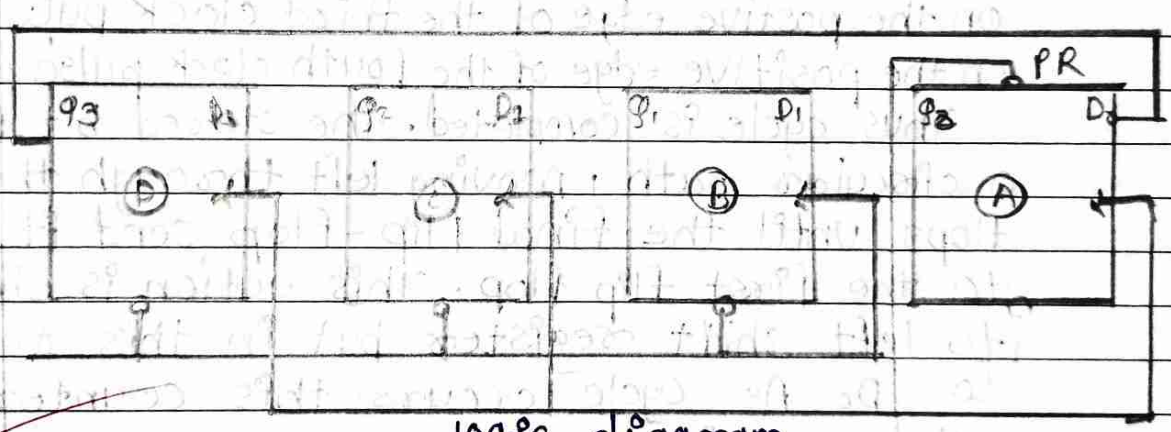
11) Explain working of 4 bit left shift resistor with logic diagram.



A group of flip flops which is used to store multiple bits of data and the data is moved from one flip flop to another data is known as shift Register. the bits stored in registers shifted when the clock pulse is applied within and inside or outside the register, we have to connect n numbers of flip flops. so, the number of bits of the binary number is directly proportional to the number of flip flops. the flip flops are connected in such a way that the first flip flop's output becomes the input of the other flip flop.

A shift Register which shifts the bit to the left, is known as "shift left register"

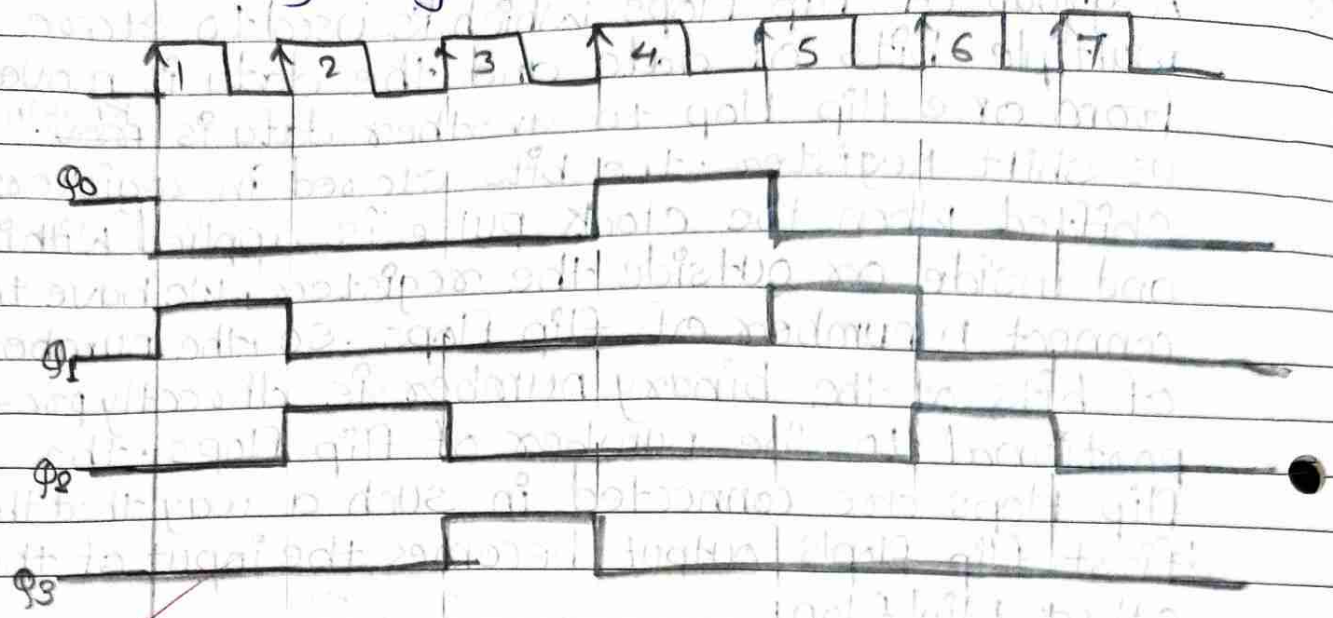
iii) Explain working of ring counter with logic diagram.




logic diagram

| $\Phi_3$ | $\Phi_2$ | $\Phi_1$ | $\Phi_0$ | |
|---|---|---|---|---|
| D | C | B | A | |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 2 |
| 1 | 0 | 0 | 0 | 3 |
| 0 | 0 | 0 | 1 | 4 |
| 0 | 0 | 1 | 0 | 5 |
| 0 | 1 | 0 | 0 | 6 |

- Timing Diagram




Ring counter can be constructed by using D flip flops. Any external data input is not applied $Q_0$ is connected to $D_1$, $Q_1$ to $D_2$, $Q_2$ to $D_3$ & $Q_3$ to $D_0$ Initia a low pulse is applied to PR input of first flip-flop Therefore, stored word becomes.

$Q = Q_3\ Q_2\ Q_1\ Q_0 = 0001$

on the postive edge of the third clock pulse $(Q) = 1000$

on the positive edge of the fouth clock pulse $= 0001$

Thus cycle is completed. the stored bit follows a circular path, moving left through the flip-flops until the final flip-flop send it back to the first flip flop. This action is similar to left shift register but in this $Q_3$ is give to $D_0$ As cycle occurs this counter is called as ring counter.

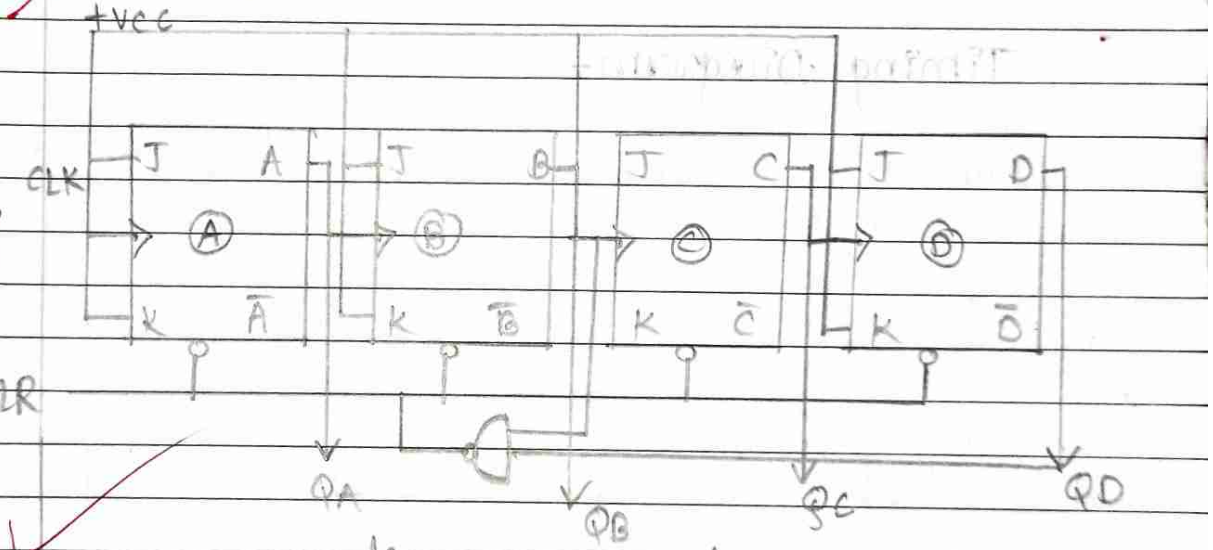
18/20

Name - Pradnya Pradip Patil.
Roll No - 7306
Std - BSC-FY Div-A

Q.1. Long answer questions.

1) Explain the decade asynchronous counter with logic diagram, truth-table and timing waveform.

→ A decade counter has modified count. By using 4 negative edge triggered J-K Flip-Flop modified 16 counter can be constructed. It has 16 states but decade counter has 10 states six states are not used. The counter must reset at the end of 10th CLK pulse feedback is used for skipping unwanted states.




Logic diagram of Decade counter

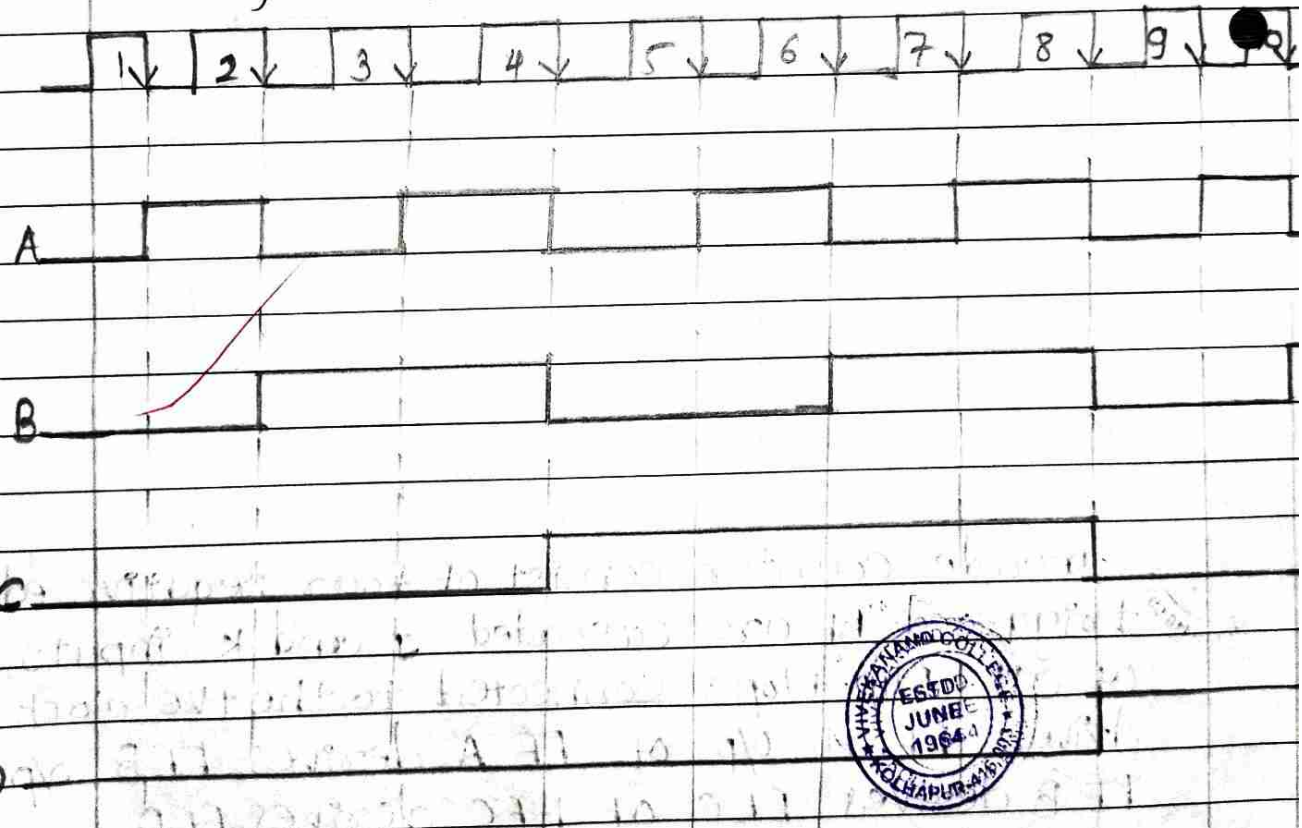
Decade counter consist of four negative edge triggered FF are cascaded J and K inputs of all flip-flops connected to the +ve clock drives FF H. O/p of FF A derives FFB o/p of FF B derives FFC of FFC derives FFD.
On the negative edge of the 10th clock pulse, A changes from 1 to 0 therefore B changes from 0 to 1.

This being a positive change flip-flops C and D are not affected. ∴ DCBA = 1010 but this state is momentary state.

Truth-table-

| CLK pulse | D | C | B | A |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |

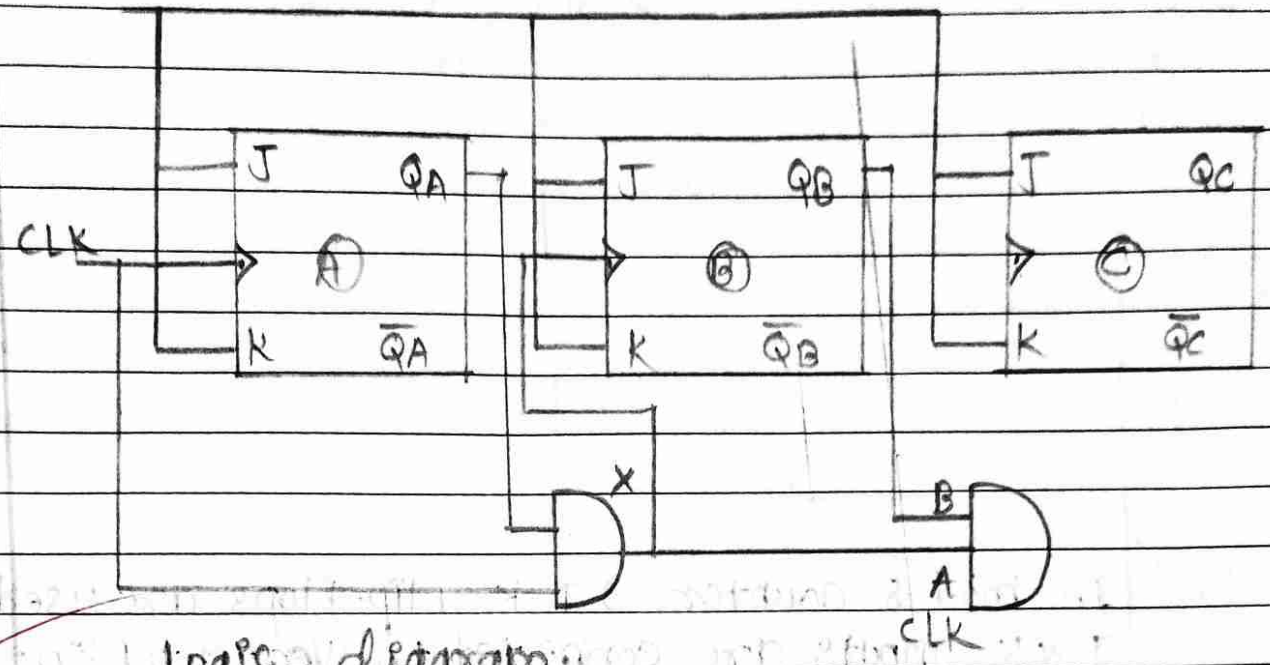
Timing Diagram-



Q.2. Short answer questions.

1) Explain Working of 3 bit synchronous counter with logic diagram, truth-table & timing waveform.

→

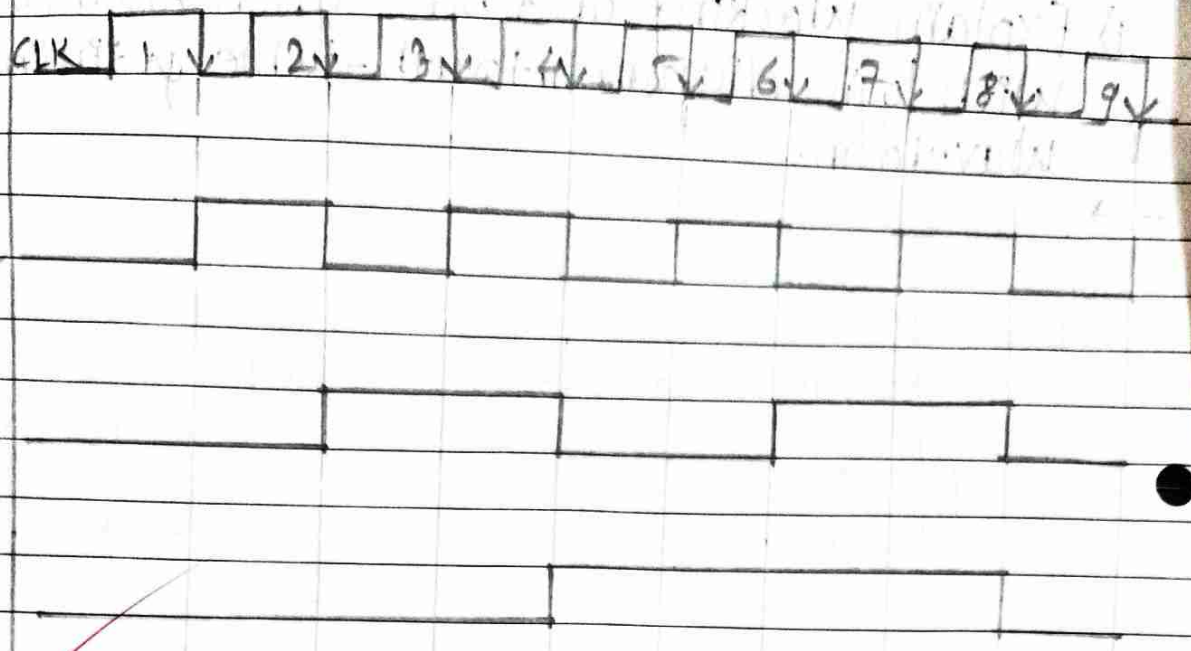



Logic diagram.

Truth-Table

| CLK Pulse | C | B | A |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |
| 8 | 0 | 0 | 0 |

Timing diagram-

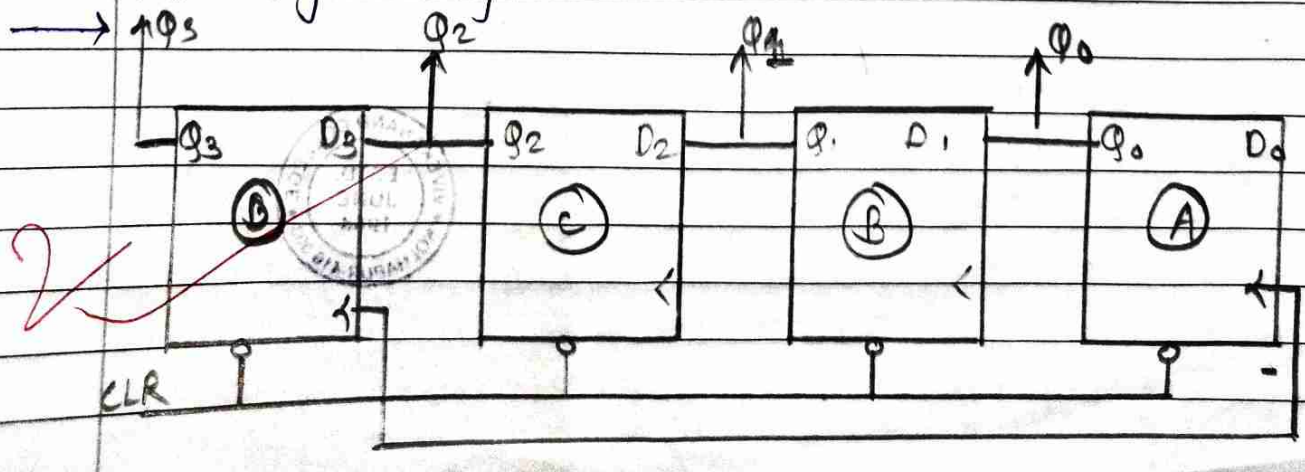



In mod-8 counter 3 J-K flip-flops are used J & K inputs are connected to +Vcc. Each flip-flop will toggle with negative clock transitions at its clock. input flip-flop A changes state with each negative clock transition whenever A is high 'X' gat is enabled. and clock pulse is passed through the gate to the clock input of flip-flop B. Thus B changes state with every second negative transition.

Thus the truth-table shows that counter progresses upwards in a natural binary sequence from count 000 upto 111.



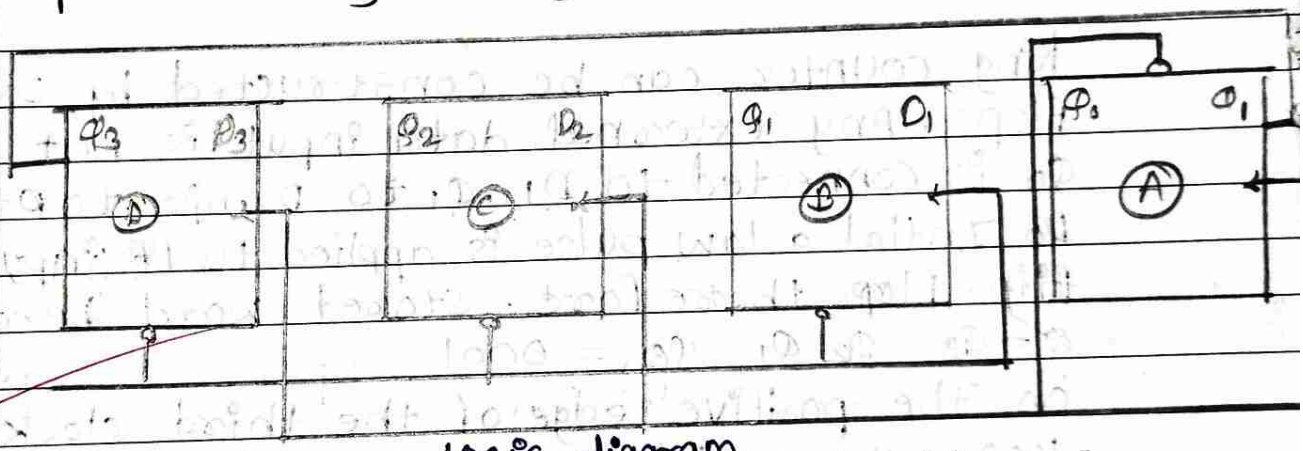
11) Explain Working of 4 bit left shift resistor with logic diagram.



A group of flip flops which is used to store multiple bits of data and the data is moved from one flip flop to another data is known as shift Register. the bits stored in registers shifted when the clock pulse is applied with in and inside or outside the register, we have to connect n number of flip flops. so, the number of bits of the binary number is directly proportional to the number of flip flops. the flip flops outputs becomes the input of the other flip flops.

A shift Register. which shifts the bit to the left is known as "shift left register"

iii) Explain working of ring counter with logic diagram



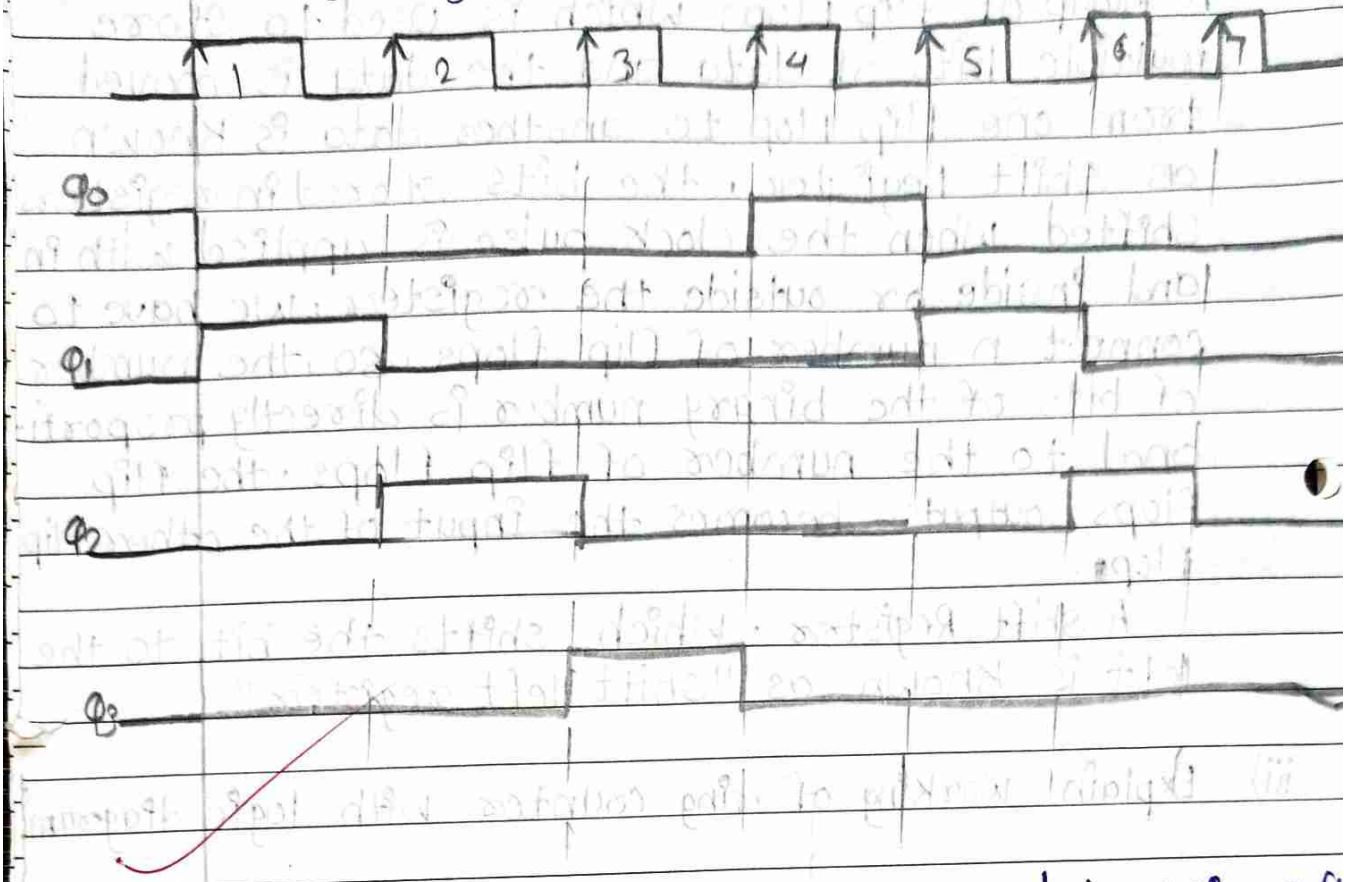

logic diagram



| $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ | |
|---|---|---|---|---|
| D | C | B | A | |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 2 |
| 1 | 0 | 0 | 0 | 3 |
| 0 | 0 | 0 | 1 | 4 |
| 0 | 0 | 1 | 0 | 5 |
| 0 | 1 | 0 | 0 | 6 |
| 1 | 0 | 0 | 0 | 7 |
| 0 | 0 | 0 | 1 | 8 |

Page No.:
Date: / /

# Timing Diagram.




Ring counter can be construsted by using D fl
flops. Any external data input is not applie
$Q_0$ is connected to $D_1$, $Q_1$ to $D_2$, $Q_2$ to $D_3$ & $Q_3$ to
$D_0$ Intial a low pulse is applied to PR input of firs
flip-flop therefore. stored word becomes.
$Q = Q_3\ Q_2\ Q_1\ Q_0 = 0001$
on the positive edge of the third clock pulse ($Q$
=1000 on the positive edge of the fouth clock pulse=00

Thus cycle is completed. the stored bit follow
a circular path, moving left through the flip-
flops ~~unti~~ until the final flip-flop send it bac
to the first flip flop. this action is similar
to left shift register but in this $Q_3$ is given
to $D_0$ As cycle occurs this counter is called
as ring counter.

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PAGE NO
DATE

Name :- Sanika S. Parpolkar
Roll No :- 7302
class :- BSC - I
Subject :- Digital Electronics - II

# Assignment

Q.1 Long answer questions.

i) Explain the decade asynchronous counter with logic diagram, truth-table and timing waveform.

A decade (mod-10) counter has modified count. By using 4 negative-edge triggered J-K flip-flop modified 16 counter can be constructed. It has 16 states but decade counter has 10 states. six states are not used (from 1010 to 1111). The counter must reset at the end of 10th CLK pulse. Feedback is used for skipping unwanted states.

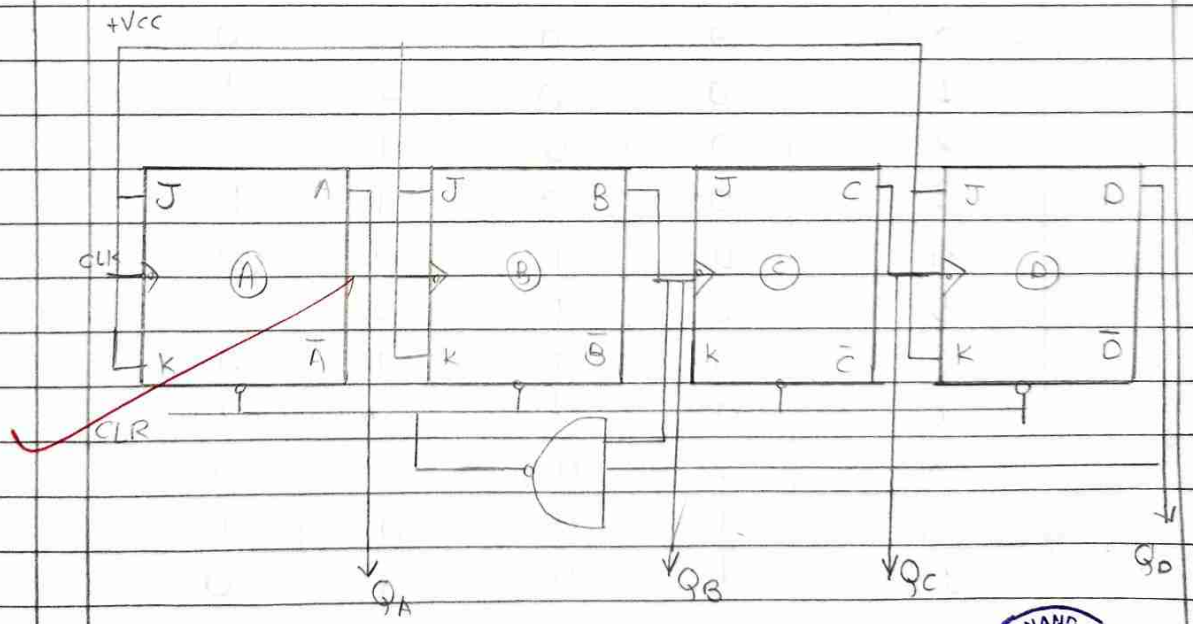


fig. Logic diagram of Decade counter

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Decade counter consist of four negative edge triggered FF are cascaded. J & K inputs of all flip-flops connected to the +vcc (logic 1). clock drives FF A. O/P of FF A drives FF B. O/P of FF B drives FF C. O/P of FF C drives FF D.

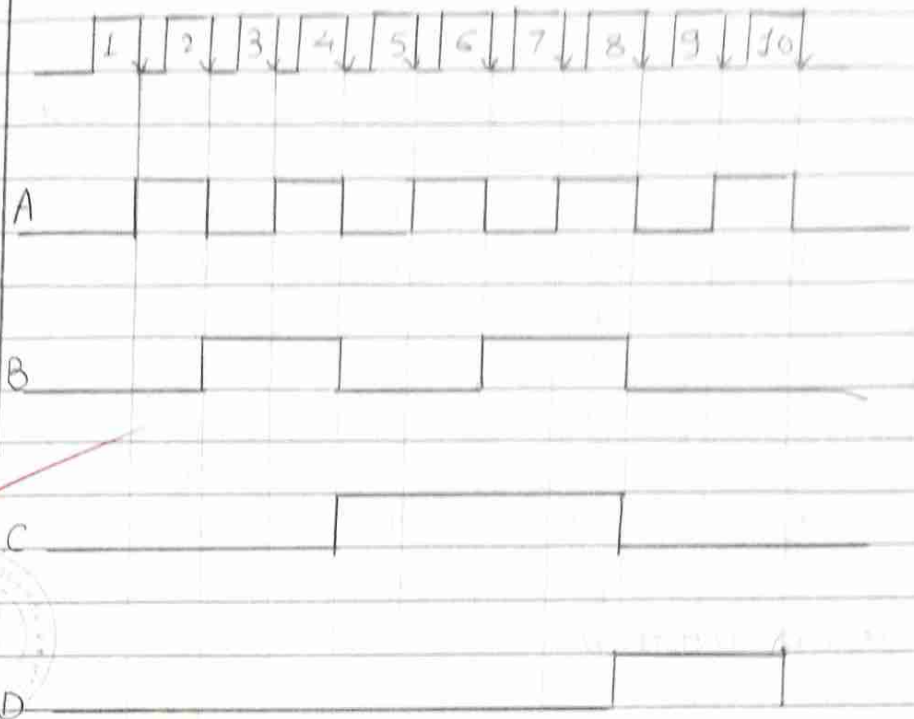
On the negative edge of the 10th clock pulse. A changes from 1 to 10 therefore B changes from 0 to 1. This ~~belong~~ being a positive change. flip-flops C & D are not affected. ∴ DCBA : 1010 but this state is momentary state.

The NAND gate provides a Reset (clear) pulse to all flip-flops as B : 1, D : 1. Because B & D are applied to NAND Gate. Therefore counter is reset & states in 16 states are skipped & it ~~loo~~ looks as decade counter.

• Truth Table

| CLK Pulse | D | C | B | A |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |

- Timing Diagram




Q.2 Short answer questions.

i) Explain working of 3 bit synchronous counter with logic diagram, truth-table & timing waveform.

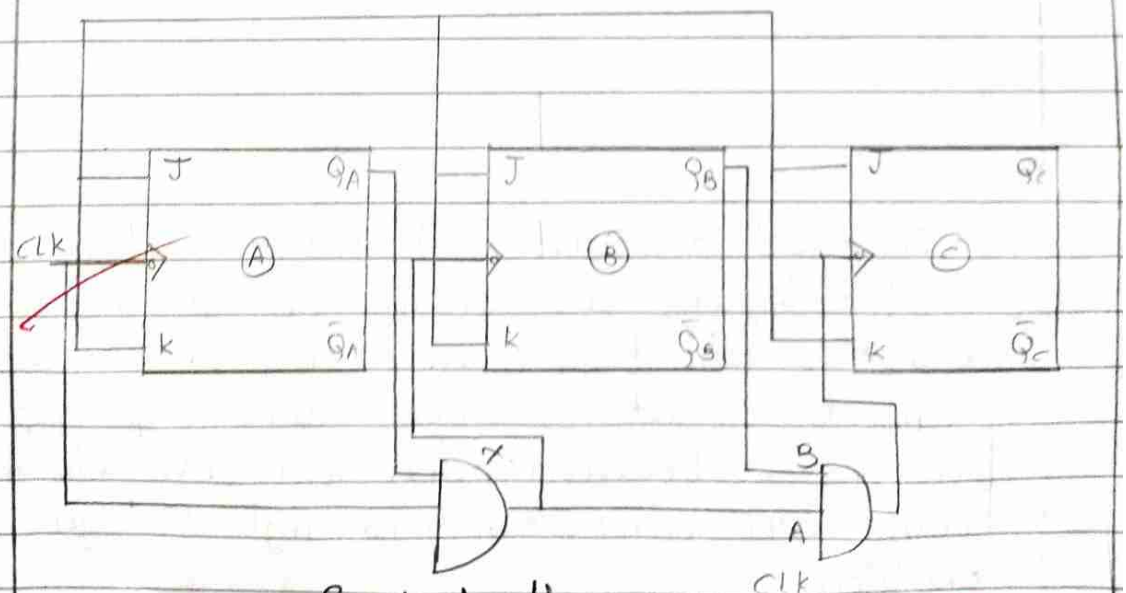



fig. Logic diagram

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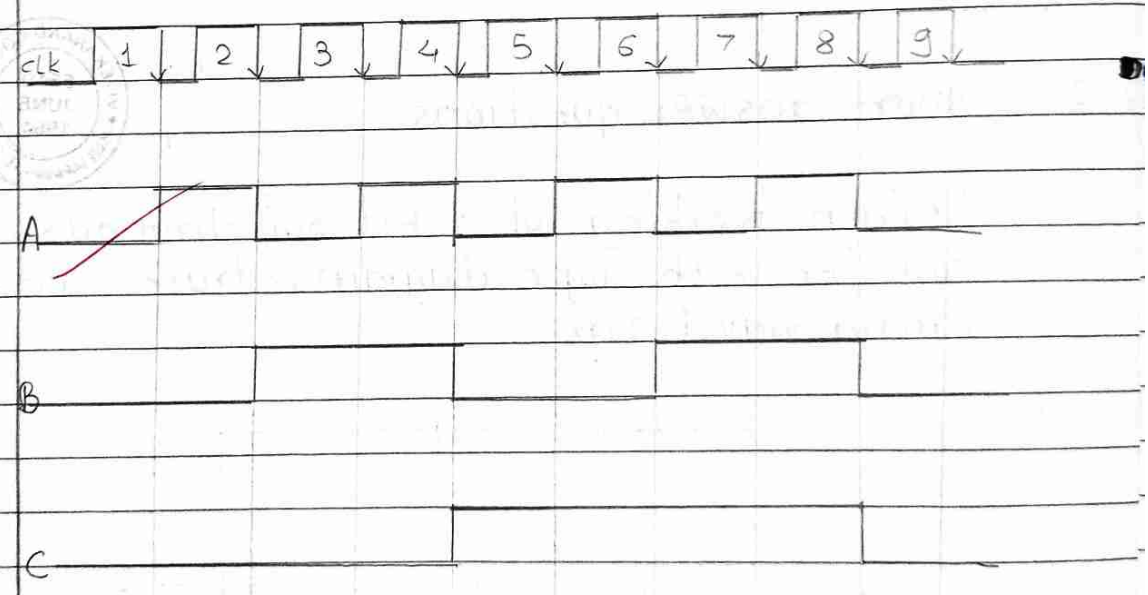
- Truth - Table

| clk pulse | C | B | A |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |
| 8 | 0 | 0 | 0 |



- Timing Diagram



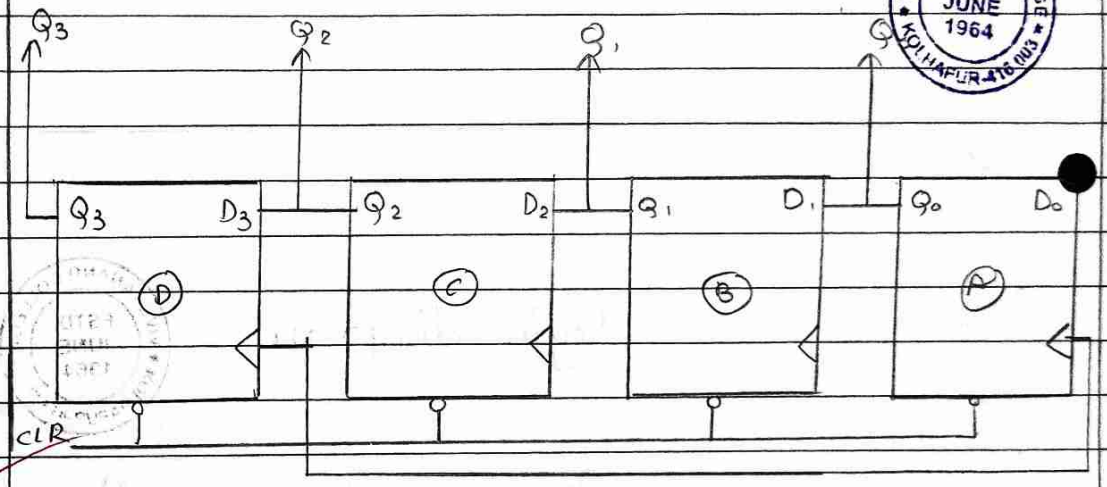

In mod - 8 counter 3 J-k flip-flops are used J & k inputs are connected to +Vcc. Each flip-flop will toggle with negative clock transitions at its clock-input. Flip-flop A changes state with each negative clock transition. Whenever A is high 'x' gate is enabled

enabled. And clock pulse is passed through the gate to the clock input of flip-flop B. Thus B changes state with every second negative transition.

Since AND gate y is enabled and will transmit the clock to the flip-flop C only when both A & B are high, flip-flop C changes state with every fourth negative clock transition.

Thus the truth-table shows that counter progresses upwards in a natural binary sequence from count 000 upto 111.

ii) Explain working of 4 bit left shift register with logic diagram.

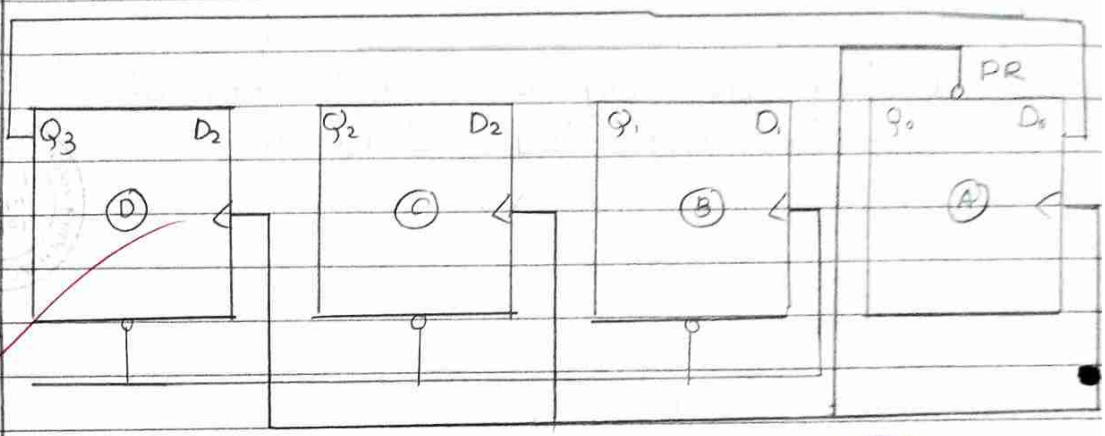



A group of flip flops which is used to store multiple bits of data and the data is moved from one flip flop to another is known as shift Register. The bits stored in registers shifted when the clock pulse is applied within and inside or outside the registers. To form a n-bit shift register, we have to connect n number of flip flops. So, the number of bits of the binary number is directly proportional to the number of flip

flops. The flip flops are connected in such a way that the first flip flop's output becomes the input of the other flip flop.

A shift Register, which shifts the bit to the left, is known as "shift left register"

iii) Explain working of ring counter with logic diagram.




Logic diagram



CLR Pulse

| $Q_3$ D | $Q_2$ C | $Q_1$ B | $Q_0$ A | |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 2 |
| 1 | 0 | 0 | 0 | 3 |
| 0 | 0 | 0 | 1 | 4 |
| 0 | 0 | 1 | 0 | 5 |
| 0 | 1 | 0 | 0 | 6 |
| 1 | 0 | 0 | 0 | 7 |
| 0 | 0 | 0 | 1 | 8 |

PAGE NO.:
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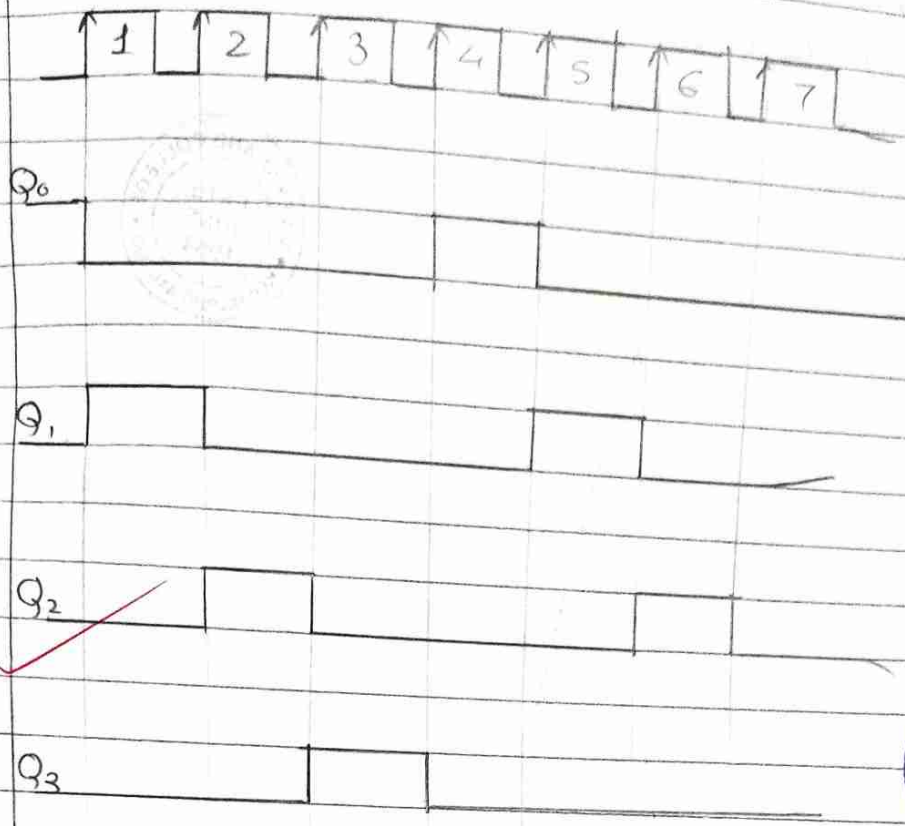
- Timing Diagram






Ring counter can be constructed by using D flip-flops. Any external data input is not applied $Q_0$ is connected to $D_1$, $Q_1$ to $D_2$, $Q_2$ to $D_3$ & $Q_3$ to $D_0$. Initially a low pulse is applied to PR input of first flip-flop. Therefore stored word becomes,

$Q = Q_3\ Q_2\ Q_1\ Q_0 = 0001$

On the positive edge of the first clock pulse (Q) : 0010. On the positive edge of the second clock pulse (Q) : 0100. On the positive edge of the third clock pulse (Q) : 1000. On the positive edge of the fourth clock pulse : 0001

Thus cycle is completed. The stored bit follows a circular path, moving left through the flip-flops until the final flip-flop send it back to the first flip-flop. This action is similar to left

shift register but in this $Q_3$ is given to $D_0$. As cycle occurs this counter is called as ring counter.