"Dissemination of education through Knowledge, Science and culture
-Shikshanmaharshi Dr. Bapuji Salunkhe

Shri Swami Vivekanand Shikshan Sanstha's

VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

Notice

(B.Sc-I Electronics) Date: 31/03/2023

All the students of B.Sc-I Electronics are hereby informed that they should write a Home assignment on Unit 1: Sequential Circuits of (Digital Electronics-II) of total 20 marks on a full scape paper and submit to the department on or before 5/04/2023.

Q.1 Long answer questions: [8 marks]

i) Explain the Master-Slave JK Flip-Flop with proper logic diagram. How it overcome the race condition of J-K flip-flop.

Q.2 Short answer questions: [4 *3=12 marks]

i) Explain working of RS Latch using NOR /NAND gates

ii) Explain working of D flip-flop with suitable diagram

iii) Explain Preset and clear concept with RS flip-flop

(Dr. P. S. Jadhav)
Subject Teacher

Dr. C. B. Patil
HEAD
DEPARTMENT OF ELECTRONICS
VIVEKANAND COLLEGE, KOLHAPUR
(AUTONOMOUS)

VIVEKANAND COLLEGE ESTD. JUNE 1964 KOLHAPUR-416 003

Shri Swami vivekanand Shikshan Santha's

VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

B.Sc . - I 2022-23

Digital Electronics

Assignment I :Unit -I Sequential Circuits

Sr. No.	Roll No.	Student Name	Assignment Submitted	Marks
1	7201	AWATI SHREYASH DILIP	Submitted	19
2	7204	KAMBLE SAURABH SANJAY	not Submitted	0
3	7207	LOKHANDE SUJAL SANDIP	not Submitted	0
4	7208	MANGAONKAR VEDANT PRASHANT	Submitted	20
5	7209	MISAL OMKAR SUNIL	Submitted	19
6	7210	MUJAWAR ZAHIR JAMIR	not Submitted	0
7	7211	NESARKAR SIDDHARTH DEEPAK	Submitted	20
8	7214	PATIL HARSHAD RAJGONDA	not Submitted	0
9	7219	SHELAKE RUPALI	Submitted	14
9	7215	PATIL HARSHVARDHAN DHANANJAY	not Submitted	0
10	7223	WARANGE NIRAJ RAJESH	Submitted	20
11	7224	YADAV HARSH NIVAS	not Submitted	0
12	7229	BHADARAGE ABHISHEK SUNIL	Submitted	20
13	7279	ALANBAGI AHMED QASIM HASAN	Submitted	15
14	7281	ASANEKAR YASH TUKARAM	Submitted	20
15	7282	BAMANE SAHIL NIVRUTI	not Submitted	0
16	7283	BAVACHE SHRAVANI BHIMRAV	Submitted	17
17	7284	CHOUGULE SAI CHANDRAKANT	Submitted	16
18	7285	CHOUGULE VAIBHAVI JAYSING	Submitted	17
19	7286	DHUMALE SANIKA SANTOSH	Submitted	20
20	7287	GHUMAI DHIRAJ BABASO	not Submitted	0
21	7288	GURAV SANIKA RAVINDRA	Submitted	20
22	7289	HIRDEKAR SHREYA SHASHIKANT	Submitted	20
23	7291	KANGRALKAR GAYATRI GUNDU	not Submitted	0
24	7292	KUMBHAR DIKSHA YUVRAJ	Submitted	16
25	7293	KUMBHAR PRATHMESH YUVRAJ	not Submitted	0
26	7294	KUMBHAR SANIKA SANJAY	Submitted	16
27	7296	MANE AARATI PRAKASH	not Submitted	0
28	7297	MANE ADITYA SHARAD	Submitted	18
29	7299	NANAVARE ADARSH VIJAY	Submitted	19
30	7301	NIMBALKAR SAIRAJ NANDKUMAR	Submitted	18
31	7302	PARPOLKAR SANIKA SUBHASH	Submitted	19
32	7303	PATIL ADITYA MANSING	not Submitted	0
33	7304	PATIL KIRTI SAMBHAJI	Submitted	18
34	7305	PATIL POONAM NARSU	Submitted	17
35	7306	PATIL PRADNYA PRADIP	Submitted	16
36	7307	PATIL PRATHAMESH BHAGAVAN	Submitted	17

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37	7308	PATIL RAVIRAJ BAJIRAO	not Submitted	0
38	7309	PATIL RIYA NITIN	Submitted	19
39	7310	PATIL SAHIL VISHNU	Submitted	20
40	7311	PATIL SAMARTH SHRIKANT	Submitted	19
41	7312	PATIL SAMMED DHANYAKUMAR	not Submitted	0
42	7313	PATIL SOURABH BHAGAWAN	not Submitted	0
43	7314	PHADAKE SUMIT RAMBHAU	not Submitted	0
44	7317	SAWANT PRATHAM PRADEEP	Submitted	19
45	7318	SHETE ANUSHKA SUNIL	Submitted	20
46	7319	SURVE VIKRANT RAJENDRA	Submitted	20
47	7320	TIWADE KETAN GIRISHKUMAR	Submitted	20
48	7325	GHODE VAISHNAVI SHRIKANT	Submitted	19
49	7332	LAMBE SANKET JAYKUMAR	Submitted	20
50	7333	LOLAGE GAYATRI GAJANAN	Submitted	20
51	7344	PATIL SHARVARI KULDEEP	Submitted	19
52	7550	DADDIKAR GAURAV NITIN	not Submitted	0
53	7551	ALTEKAR ADITYA MAHESH	Submitted	20
54	7563	AHMED SAMI ALITTIBIN	Submitted	20
55	7567	PATIL SWAPNIL SURESH	Submitted	20
56	7569	SHINDE RUGVED TANAJI	not Submitted	0
57	7584	PATIL PRATHMESH KALLAPPA	Submitted	19

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Dr. P.S.Jadhav

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VIVEKANAND COLLEGE ESTD. JUNE 1964 KOLHAPUR-416 003

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Class :- FY BSC
Roll No :- 7223 Div :- A

20/20

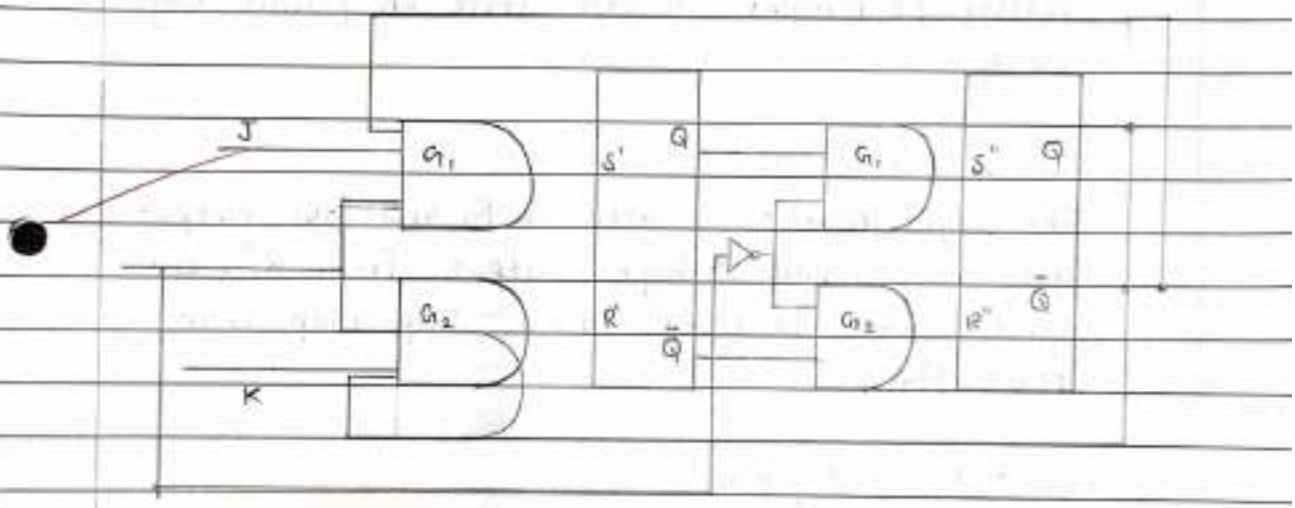
Goodluck | Page No.
Date

Assignment.

Q1. long answer questions.

i). Explain the Master-Slave JK Flip-Flop with proper logic Diagram. How it overcome the race condition of J-K Flip-Flop.

→



J-K master slave Flip-Flop consists of two J-K Flip-Flops. First is called the master which is positive edge triggred & second is called the slave which is negative edge triggered.

master Flip-Flop responds to I/P's J & K I/p's when clock is positive edge triggred. Slave Flip-Flop responds to the J & K when it is negative edge triggered.

Goodluck

Truth Table :

CLK	J	K	Q_{n+1}	Action
0	X	X	Q_n (LS)	No change
1	0	0	Q_n (LS)	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\overline{Q_n}$	Toggle

Working

Case I : J = K = 0

With both inputs at logic 0 $S_1 = 0$, $R_1 = 0$ O/P of master FF remains in last state on positive edge of clock.

Case II : J = 0, K = 1

The high input K = 1 goes to R_1 and low output goes to S_1. Due to high output from R_1 clock forces Slave to reset. Hence Flip-Flop is in reset state.

Case III : J = 1, K = 0

The high input J = 1 goes to S_1 and low input K = 0 goes to R_1. Due to high output from S_1 clock forces Slave to set. Hence Flip-Flop is in reset state.

Case IV : J = 1, K = 1

When J = 1 and K = 1 the output toggles on the positive transition of the clock and the Slave toggles on the negative transition of the clock.

In the case of J-K Flip-Flop when J=1, K=1 the o/p toggles between 0 & 1 as the clock remains high under such condition o/p is unpredictable this condition is called as race around condition. This is drawback of J-K Flip-Flop.

This can be avoided by:

i] Increasing the propagation delay time more than the clock plus width.

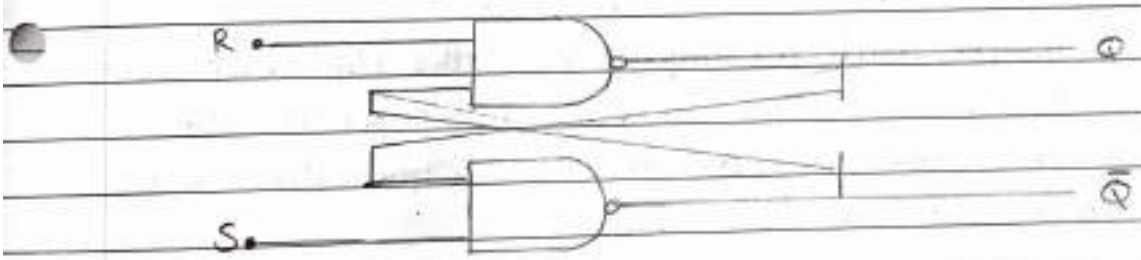
ii] Triggering the Flip-Flop on clock edges.

iii] Isolating I/p & o/p of J-K Flip-Flop.

Q 2. Short answers questions:

1). Explain working of RS latch using NOR / NAND gates

a] R-S Flip-Flop using NAND Gate:



RS Flip-Flop using NAND gate consists of two NAND gates G_1 & G_2 in which output one is given to the I/p of other.

In case of NAND gate if one of the I/p is low the o/p is high.

Truth Table:

R	S	Q	action
0	0	Forbidden	Race
0	1	1	Set
1	0	0	Reset
1	1	L.S	No change

Working :

Case I : When R = 0, S = 0

With the R = 0 & S = 0 the output G_1 & G_2 goes high i.e $Q = \bar{Q} = 1$ but this is not allowed because Q & $\bar{Q}$ are always complementary. This state is called as forbidden state.

Case II : When R = 0, S = 1

With R = 0 the output of NAND gate G_1 become Q = 1, S = 1, the output of NAND gate G_2 $\bar{Q} = 0$ this condition is called as setting the Flip-Flop.

Case III :- When R = 1, S = 0

With R = 1, S = 0 the output of NAND gate G_2, $\bar{Q} = 1$ as $Q = \bar{Q}$ are always complementary $Q = 0$.

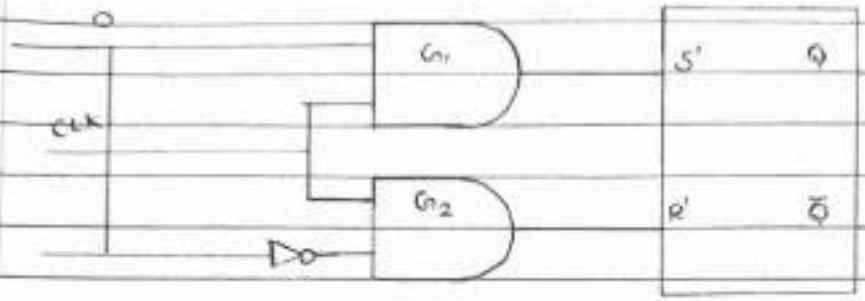
This is called as resetting the Flip-Flop

Case IV :- When R = 1, S = 1

With the both the inputs high the Flip-Flop does not change its state because 1 I/P at the input of NAND has no effect on the output thus o/p remains in the last state.

Suppose last state is $Q = 1$ & $\bar{Q} = 0$, & I/P's to the NAND gate are R = 1, S = 1 then the output remains unchanged.

ii). Explain working of D Flip-Flop with suitable diagram.



logic Diagram.

A D Flip-Flop or D latch is level clocked. It consist of R-S Flip-Flop, two AND gates & a NOT Gate.

Truth table :

CLK	D	Qn+1	Action
0	X	last state	No change
1	0	0	Reset
1	1	1	Set

Working :

In case of AND gate if one of input in low output is low.

Case I : When CLK is low (0):

when clock (CLK) is low both AND gates are disabled so D is in Don't care condition (x) i.e. 0 or 1

∴ o/p is in last state

∴ $Q_{n+1} = Q_n$

Case II : when CLK is high o/p depends upon the data I/P 'D'.

a) D = 0

When D = 0 upper AND gate provides low output & lower AND gate provides high output.

ie. S = 0, R = 1 therefore o/p is in low state.

$\therefore Q_{n+1} = 0$

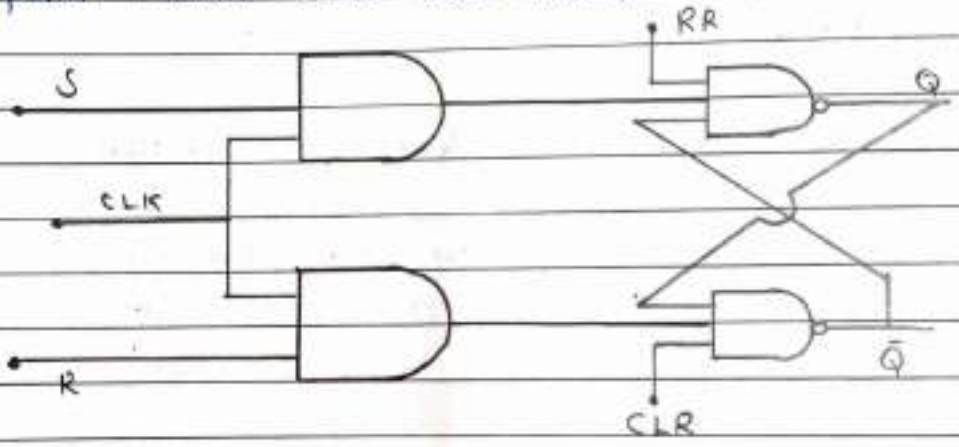
b) D = 1

When D = 1 upper AND gate provide high output & lower AND gate provide low output ie. S = 1, R = 0 therefore o/p is high (1)

$\therefore Q_{n+1} = 1$

In D Flip-Flop the output follows the value D.

iii) Explain Present and clear concept with RS Flip-Flop.



Present and Clear Facility in RS FF:

In RS Flip Flop OR gates provides preset and clear inputs. Upper OR gate provides PRESET & lower OR gate provides CLR I/P

OR gate provides high output if any one of I/P is high.

Case 1: RR = 0, CLR = 1

When CLR = 1, lower OR gate passes reset signal

When $\therefore$ o/p $Q_{n+1} = 0$

Here CLR, R & S are don't care condition

Truth table :

PR	CLR	CLK	R	S	Q_{n+1}	
0	1	X	X	X	1	Action
1	0	X	X	X	0	set
1	1	0	X	X	Q_n (LS)	Reset
1	1	1	0	0	Q_n (LS)	No change
1	1	1	0	1	1	No change
1	1	1	1	0	0	
1	1	1	1	1	Forbidden	

In case of NAND gate ; if one of the I/p is low O/P is high

Working :

Case I : When R = 0 , CLR = 1
when PR = 0 , CLR = 1, lower OR gate passes reset signal.
∴ output Q_{n+1} = 0 here CLR.

Case II :- When PR = 1 & CLR = 0
when PR = 1 , CLR = 0 upper OR gate passes set signal.
∴ Output Q_{n+1} = 1
Here CLK, R, S are don't care condition

Case III : When PR = 0 , CLR = 0 & CLK = 1
The action is similar to normal clocked RS - Flip - Flop.

Case IV : When PR = 0 CLR = 0, CLK = 0
output remains in the last state R & S
In don't care condition.
PR = 1, & CLR = 1 not allowed it causes
race condition.

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Q.1 Long answer Questions.

i Explain the Master-slave Jk Flip-Flop with proper logic diagram. How it overcome the race condition of J-k Flip-Flop.

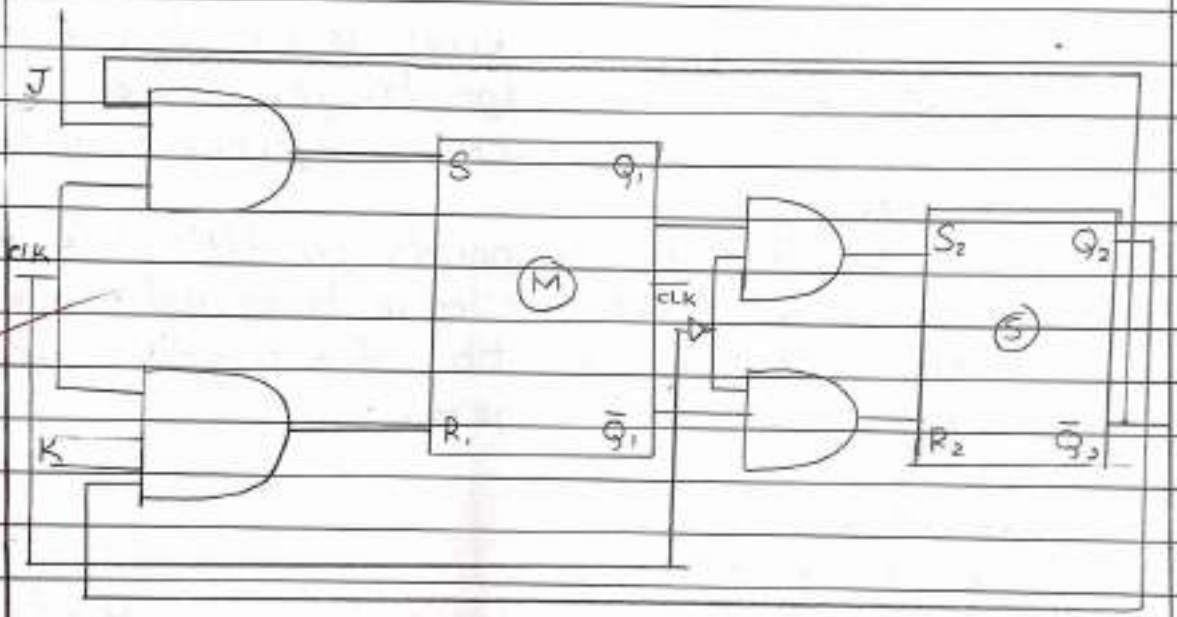

fig. logic diagram of J-k Flip-Flop

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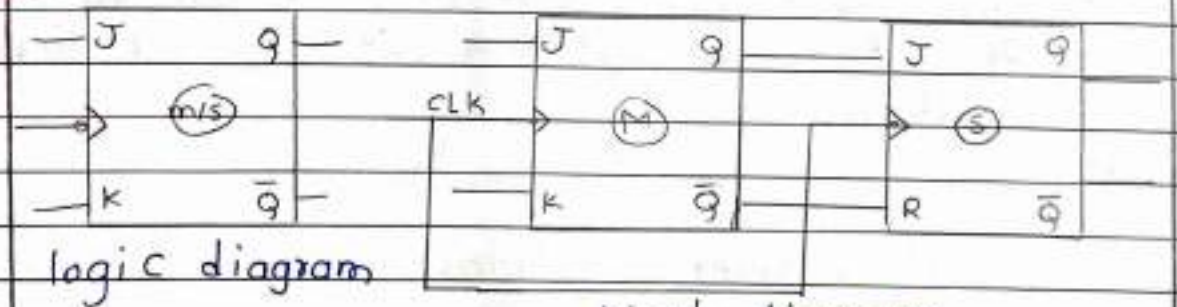


logic diagram

block diagram

Goodluck

Truth-Table.

Clk	J	K	Q	Action
0	X	X	Q_{n+1}	NC
↓	0	0	Q_n (LS)	NC
↓	0	1	0	Reset
↓	1	0	1	set
↓	1	1	$\bar{Q}_n$	Toggels

J-K master slave flip-flop consists of two J-K flip-flops first is called the master which is positive edge triggered & second is called the slave which is negative edge triggered.

Master flip-flop responds to I/P's J & K I/P's when clock is positive edge triggered. Slave flip-flop responds to the J & K I/P's when it is negative-edge triggered.

Working:-

Case I:- J = K = 0

With both inputs at logic '0' ∴ $S_1 = 0$, $R_1 = 0$ o/p of ~~mat~~ master FF. remains in the last state on positive edge of clock. Due to this S_2 & R_2 of second R-S flip-flop remains constant.

Q.2 Short answer questions

i Explain working of RS & flip-flop latch using NOR/NAND gates.

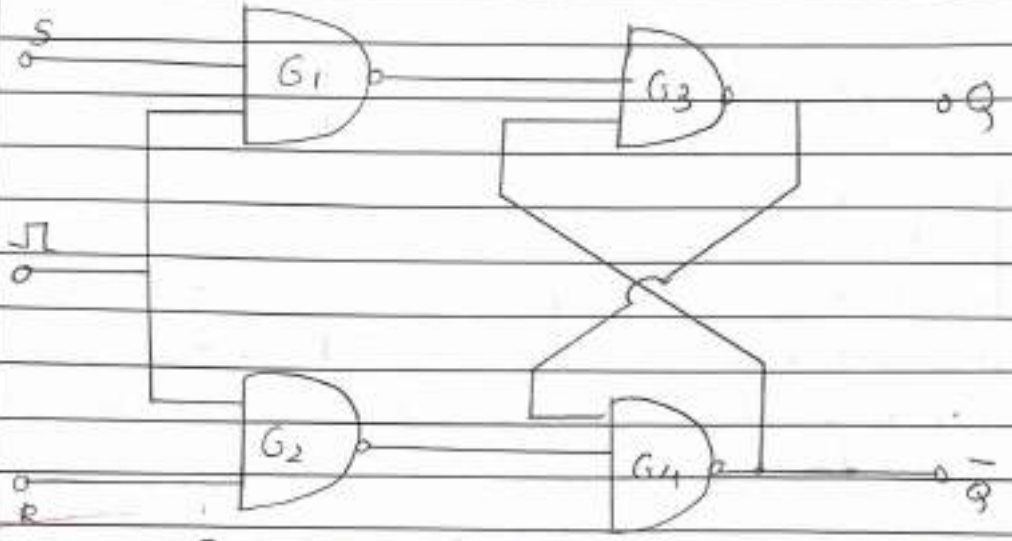


fig: Logic diagram of R-S FF using NAND Gate

- Truth-table

Inputs			Output
clk	R	S	Q_{n+1}
0	x	x	Q_n (LS)
1	0	0	Q_n (LS)
1	0	1	1 (set)
1	1	0	0 (Reset)
1	1	1	forbidden

The NAND gate is a gate in which if one of the input is low the output is high.

Working:

case I) When clk is 0 (LOW):- When clk is low the outputs of NAND G_1 & G_2 are high. But with high inputs the NAND gates G_3 & G_4 does not responds. It does not changes its state.

O/P $Q_{n+1} = Q_n$ i.e O/P after the clock pulse

is equal to the clock before the clock pulse.

case II) When clk is high (1)
When clk is high output depends on R & S inputs.

a) R = 0, S = 0
with R = 0, S = 0 the O/P's of NAND Gate G_1 & G_2 are high, But with high input gate G_3 & G_4 does not change their state therefore output remains in the last state.
$\therefore Q_{n+1} = Q_n$

b) R = 0, S = 1
with R = 0 & S = 1 the upper NAND gate G_1 provides low output & lower NAND gate G_2 provides high output with low input NAND Gate G_3 provides high output $\therefore Q_{n+1} = 1$

c) R = 1, S = 0
with R = 1 & S = 0 the upper NAND gate G_1 provides high output & lower NAND gate G_2 provides low output with low input NAND gate G_4 provides high output ($\bar{Q}$) as Q & $\bar{Q}$ are always complementary $Q = 0 \therefore \bar{Q} = 1$
$Q_{n+1} = 0$

d) R = 1 & S = 1
with R = 1 & S = 1 the output of NAND Gate G_1 & G_2 are low therefore inputs of the NAND Gates G_3 & G_4 are low this makes Q = 1 & $\bar{Q} = 1$. Q & $\bar{Q}$ are always complementary. This state is allowed state which is called as forbidden state.

ii Explain working of D flip-flop with suitable diagram.

The R-S flip-flop has two disadvantages
a) To store a high(1) bit, high 'S' is headed & store low(0) bit high 'R' is needed.
b) If R=1, S=1 the output is in forbidden state this state should be avoided as occures.

These drawbacks can be removed by using a D flip-flop (D latch)

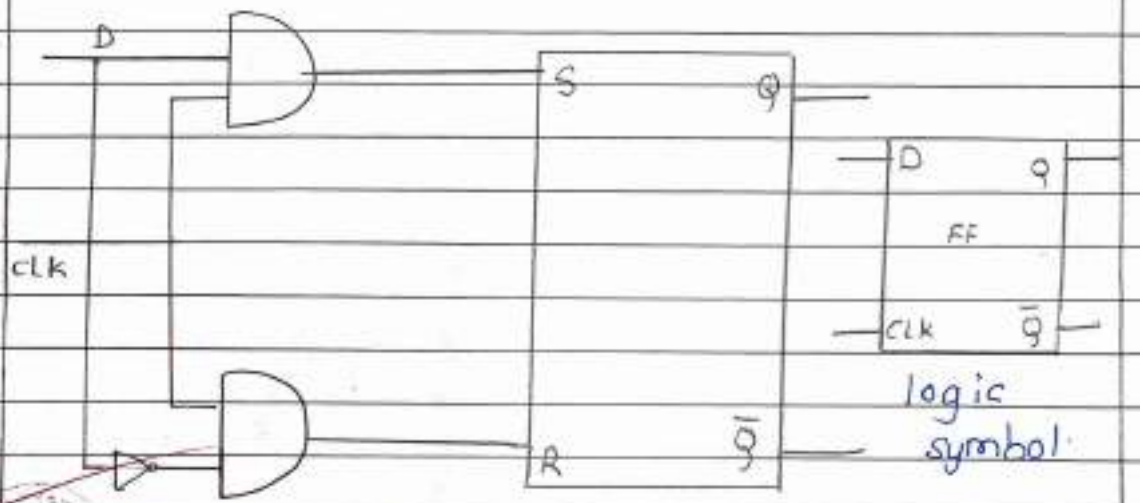


fig. logic diagram

04 A D flip-flop or D latch is level clocked. It consist of R-S flip-flop, two NAND Gates & a NOT Gate.

Working :- In case of AND gate if one of input is low output is low.
case I) When clk is low (0)
When clk is low both AND gates are disabled so D is in Don't care condition (x) i.e 0 or 1.
∴ o/p is in last t state ∴ $Q_{n+1} = Q_n$ i.e last state.

Case II] When clk is high O/P depends upon the data I/P 'D'

a) D = 0

When D = 0 upper AND gate provides low output & lower AND provides high output i.e S = 0, R = 1 therefore O/P is in low state

$\therefore Q_{n+1} = 0$

b) D = 1

upper AND gate provide high output & lower AND gate provide low output i.e S = 1, R = 0 therefore O/P is high (1)

$\therefore Q_{n+1} = 1$

In D flip-flop the output follows the value D.

Truthtable

Inputs		output
clk	D	Q_{n+1}
0	x	Q_n (LS)
1	0	0
1	1	1

iii) Explain Preset and clear concept with RS flip-flop.

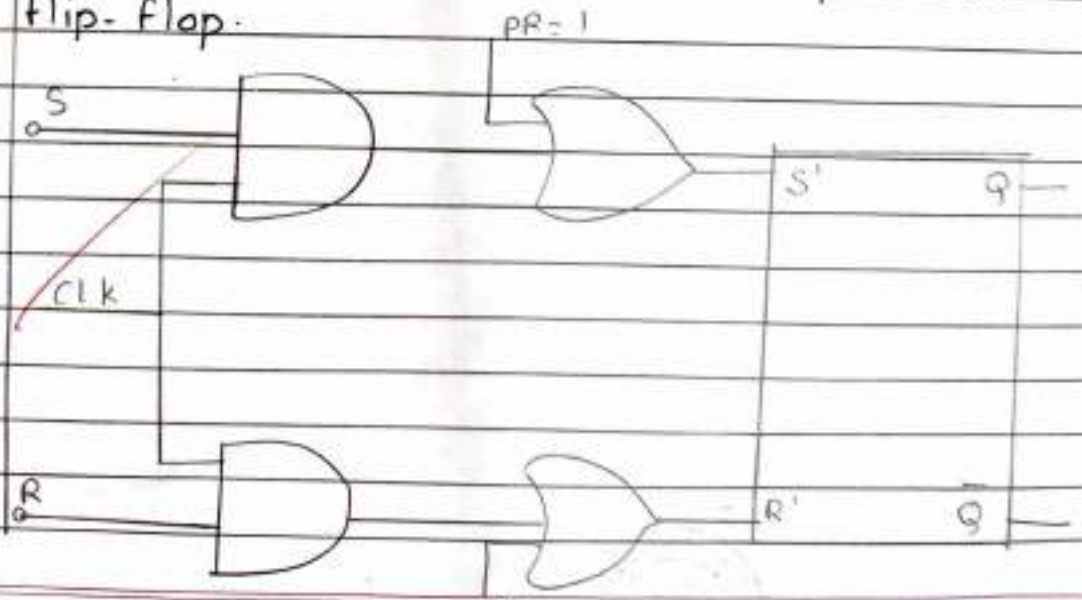
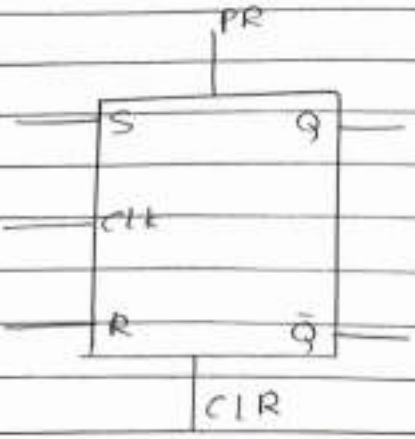


fig: Logic diagram



Logic Symbol

OR gates provides presets & clear inputs
upper OR gate provides PRESETS & lower OR gate provides CLR I/P
OR gates provides high output if any one of the I/P is high.

Case I) PR = 0, CLR = 1
When CLR = 1, lower OR gate passes reset signal.
∴ o/p $Q_{n+1} = 0$ Here clk, R & S are don't care condition

Truth - Table

			I/P	O/P
PR	CLR	Clk	D	Q_{n+1}
0	0	0	x	Q_n (Ls)
0	0	1	0	0
0	0	1	1	1
1	0	x	x	1
0	1	x	x	0

Working:-

Case I) When PR = 0, CLR = 0 & CLK = 0
Control I/P's does not reach the flip-flop therefore flip-flop output remains in the last state
∴ $Q_{n+1} = Q_n$ & D is in Don't care

Case II) When PR = 0, CLR = 0 & CLK = 1
The flip-flop work as normal clocked D-flip flop

Case III) When PR = 1, CLR = 0
The upper OR gate provides set signal
∴ $Q_{n+1} = 1$
∴ CLK, D I/P's are don't care

Case IV) When PR = 0 & CLR = 1
The lower OR gate provides Reset signal.
∴ O/P $Q_{n+1} = 0$
∴ CLK, D ~~I/Ps~~ are don't care condition
PR = CLR = 1 not allowed it causes race condition
Thus when PR = 1 the output flip-flop is in set condition when CLR = 1 the O/P of flip-flop is in Reset condition.

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GoodLuck | Page No. | Date

Name :- Shewari Kuldeep Patil
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Q1. Long answer questions : [8 marks].

i] Explain the Master-Slave JK Flip-Flop with proper logic diagram. How it overcome the race condition of J-K flip-flop.

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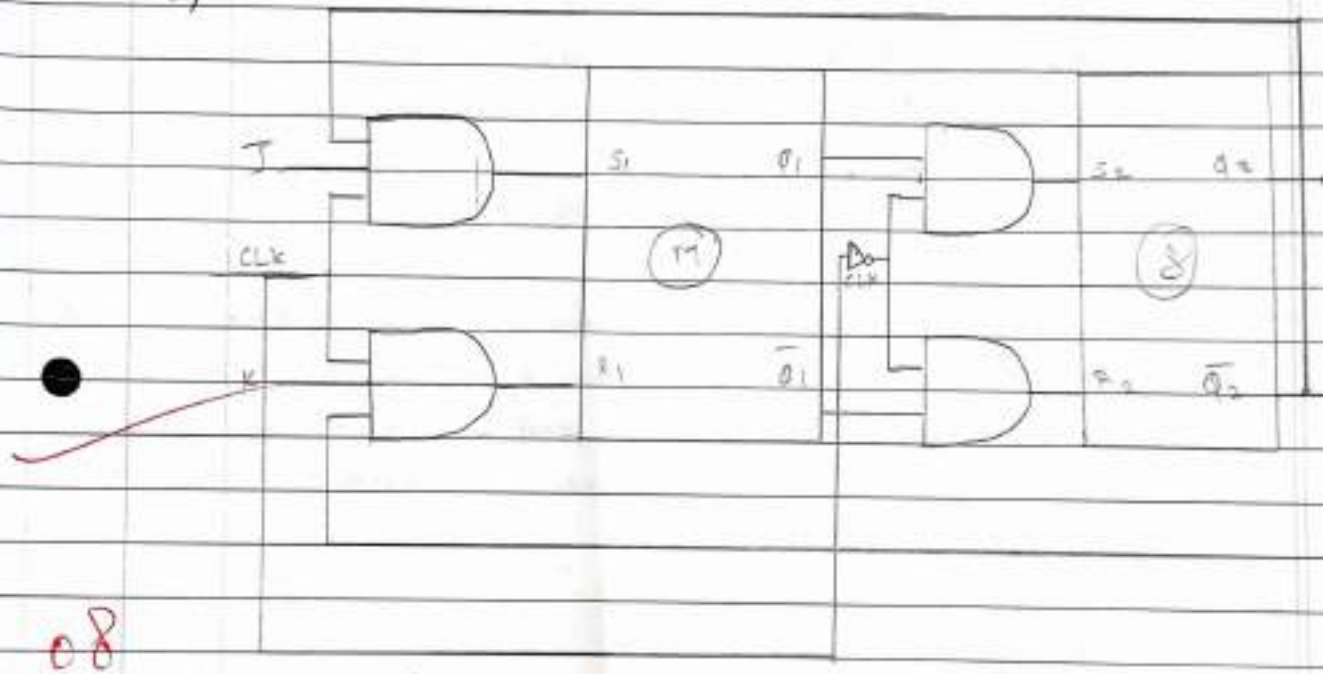

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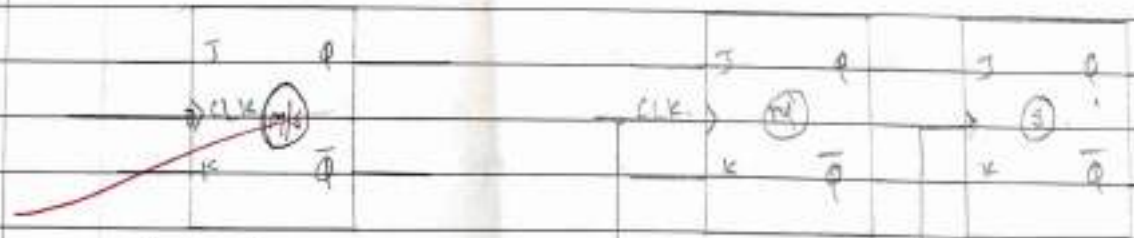


logic diagram

block diagram.

J-K. master slave flip-flop consists of two J-K flip-flops first is called the master is positive edge triggered & second is

called the slave which is negative edge triggered.
Master flip-flop responds to I/P's J & K I/P's when clock is positive edge triggered slave flip-flop responds to J & K I/P's when it is negative-edge triggered.

Working :-

Case I :- J = K = 0.
with both Inputs at logic '0' ∴ $S_1 = 0$, $R_1 = 0$ O/P of master FF remains in last state on positive edge of clok. Due to this S_2 & R_2 of second R-S flip-flop remains unchanged hence slave O/P remains in the last state.

Case II :- J = 0, K = 1
$S_1 = 0$, $R_1 = 1$ on leading edge master ff resets.
∴ $\phi_1 = 0$, $\bar{\phi}_1 = 1$ Now I/P's $S_2 = 0$ & $R_2 = 1$ on falling edge. slave ff ~~sets~~ ∴ ~~$\phi_2 = 1$ $\bar{\phi}_2 = 0$.~~
(or on -ve edge) slave ff resets.
$\phi_2 = 0$, $\bar{\phi}_2 = 1$.

Case III :- J = 1, K = 0
with J = 1, $S_1 = 1$, $R_1 = 0$ on leading edge master ff sets.
∴ $\phi_1 = 1$, $\bar{\phi} = 0$ Now I/P's $S_2 = 1$ & $R_2 = 0$.
Falling edge slave ff sets $\phi_2 = 1$ $\bar{\phi}_2 = 0$.

Case IV :- J = 1, K = 1.
with both inputs high ϕ_1 & $\bar{\phi}_1$ toggle on leading edge of clock (i.e master ff toggles) while slave ff toggles on falling edge of clock.

Case III :- When S=1, R=0.

When S=1, R=0 the O/P of G2 i.e $\bar{Q}=0$ as Q & $\bar{Q}$ are complementary ∴ Q=1.

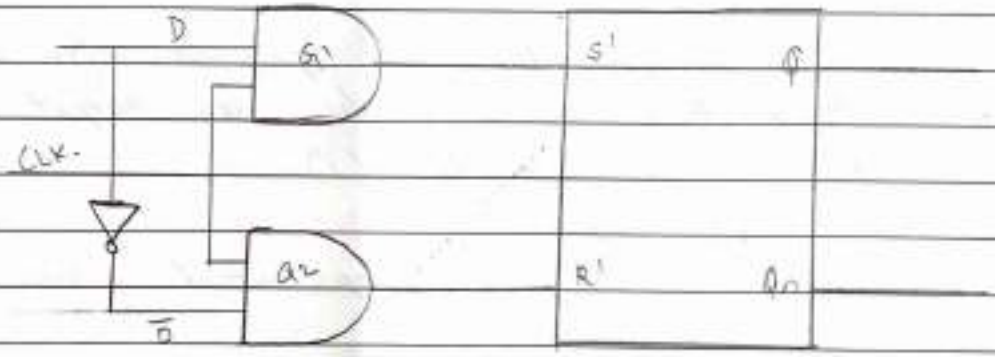
The condition is called as setting the flip-flop.

Case IV :- When S=1, R=1.

When S=1, R=1 both NOR gate try to disable. i.e simultaneously $Q=\bar{Q}=0$. This state is not allowed. This state is called as forbidden state.

2. Explain working of D-Flip-Flop with suitable diagram.

Circuit Diagram :-



Truth Table :-

CLK	D	Qn+1	Action.
0	X	last state.	No change
1	0	0	Reset
1	1	1	Set.

Working :-

In case of AND gate if one of the input is low output is low.

Case I :- When clk is low (0)

When clk is low both AND gates are disable so D is in don't care condition (x) i.e 0 or 1.

∴ O/P is in last state ∴ $Q_{n+1} = Q_n$ i.e last state.

Case II :- When clk is high O/P depends upon the data I/P D.

a) D = 0

When D=0 upper AND gate provides low output & lower AND provides high output i.e S=0, R=1 therefore OP is in low state ∴ $Q_{n+1} = 0$.

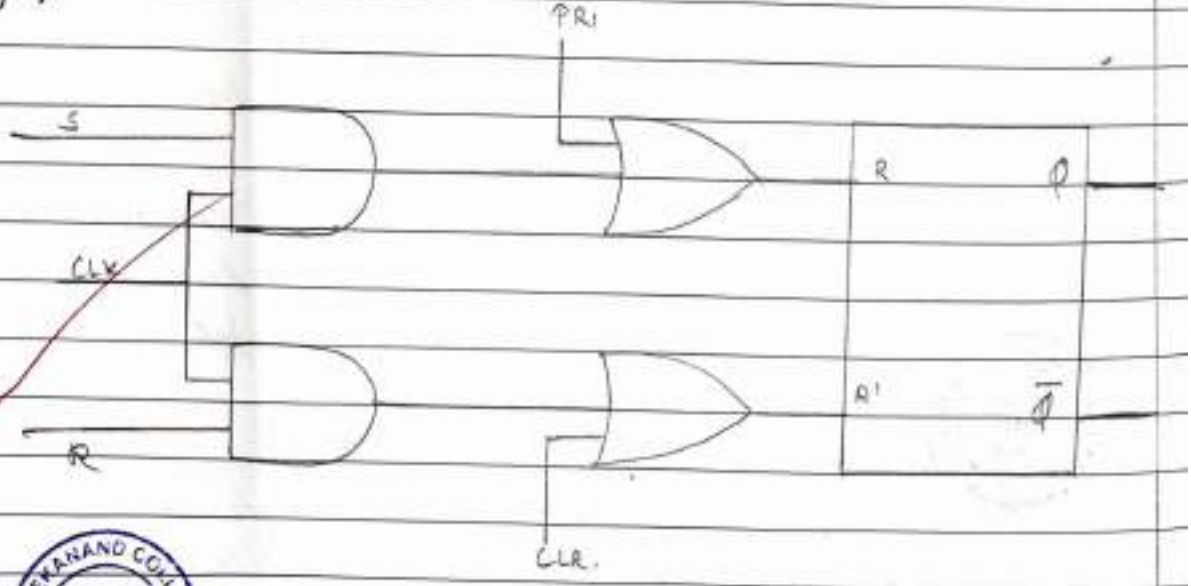
b) D = 1

Upper AND gate provides high output & lower AND gate provides low output i.e S=1, R=0 ∴ O/P is high (1).

∴ $Q_{n+1} = 1$

In D flip-flop output follows the value D.

3. Explain Preset and clear concept with RS flip-flop.



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Reset and clear facility is clocked RS flip-flop or gate provides preset and clear inputs upper or gate provides clr I/P.
OR gate provides high output if any one of I/P is high.

Case I :- $\overline{PR}=0$, $\overline{CLR}=1$.
When $\overline{CLR}=1$ lower or gate passes reset signal. ∴ O/P $Q_{n+1}=0$. Here CLK, R & S are in don't care condition.

Case II :- When $\overline{PR}=1$ & $\overline{CLR}=0$.
When $\overline{PR}=1$, $\overline{CLR}=0$ upper or gate passes set signal ∴ O/P $Q_{n+1}=1$ Here CLK R, S are don't care condition.

Case III :- When $\overline{PR}=0$, $\overline{CLR}=0$ & CLK = ↓
The action is similar to normal clocked R-S ff

Case IV :- When $\overline{PR}=0$, $\overline{CLR}=0$, $\overline{CLR}=0$
O/P remains in the last state R & S in don't care condition $\overline{PR}=1$ & $\overline{CLR}=1$ not allowed it causes race condition.

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Truth Table :-

$\overline{PR}$	$\overline{CLR}$	CLK	Inputs		Output
			R	S	Q_{n+1}
0	0	0	x	x	Q_{n+1}
0	0	1	0	0	Q_n (last state
0	0	1	0	1	Q_n (last state)
0	0	1	1	0	1
0	0	1	1	1	0
0	1	x	x	x	forbidden
1	0	x	x	x	0

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Truth Table :-

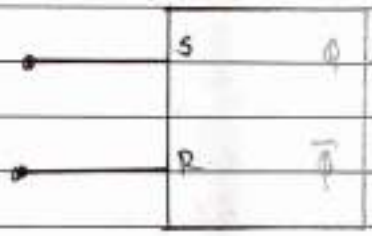
CLK	J	K	Qn+1
↓	x	x	Qn (last state)
H	x	x	Qn (last state)
↓	0	0	Qn (last state)
↓	0	1	0
↓	1	0	1
↓	1	1	Qn (last state) (toggle)

Q2 Short answer questions :-

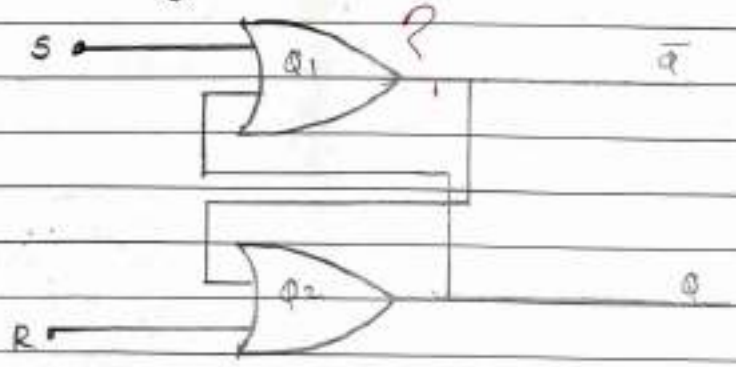
1. Explain working of Rs latch using NOR/NAND gate.

R-S latch using NOR gate :-

Block diagram :-



Circuit diagram :-



Truth table :-

Inputs		Output		Action
S	R	Q	$\bar{Q}$	
0	0	last state	last state	No change.
0	1	0	1	Reset
1	0	1	0	Set
1	1	0 (forbidden)	0 (forbidden)	forbidden.

Working :-

R-S flip-flop using NOR can be constructed as shown in diagram in which output of one gate is given to input of other gate.

In case of NOR gate if one of the input is high then output becomes low.

Case I :- When S=0, R=0.

When there is a 0 at the input of the NOR it do not have any effect on the output so output remains in the last state.

If the O/P $\phi=1$ & $\bar{\phi}=0$ if the input to flip-flop are R=0, S=0 then o/p remains in the last state $\phi=1$.

Case II :- When S=0, R=1.

When S=0 & R=1 then O/P of G, i.e $\phi=0$ it causes $\bar{\phi}=1$. The condition $\phi=0$ is called as resetting the flip-flop.

'19/20

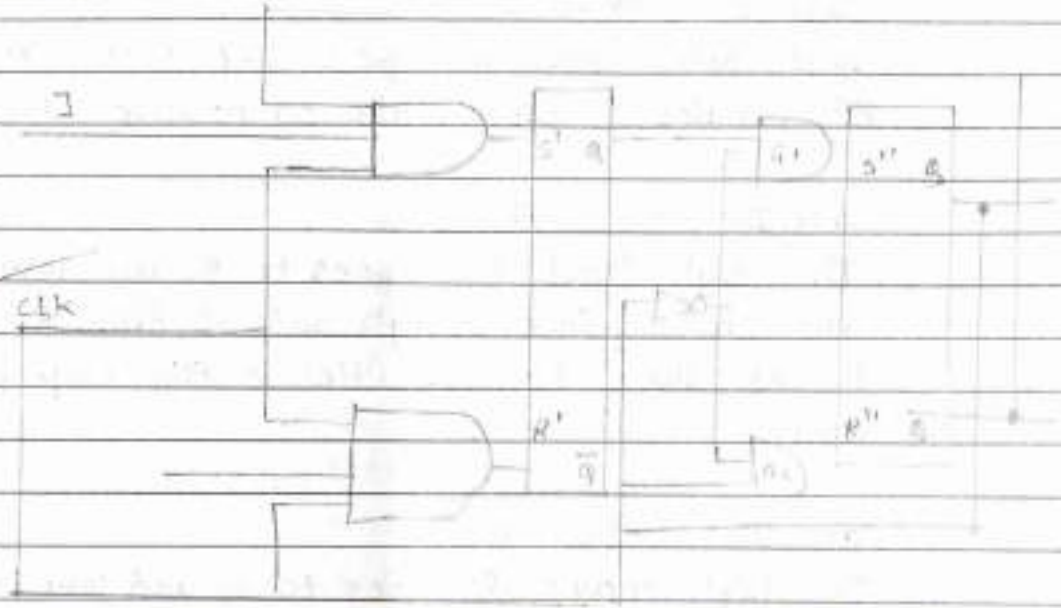
Name: Riya Nitin Patil
Div: A class: BSC. FY
Roll NO: 7309

Assignment

Q1 Long answer question:

i] Explain the master-slave JK flip-flop with proper logic diagram. How it overcome the race condition of J-K flip-flop.

→



J-K master slave flip-flop consists of two J-K flip-flops first is called the Master which is positive edge trigged & second is called the slave which is negative edge triggered.

master flip-flop responds to I/P's J & K I/P's when clock is positive edge triggred slave flip-flop responds to the J & K when it is negative edge triggered.

Truth table:

CLK	J	K	Q_{n+1}	Action
0	x	x	Q_n (LS)	No change
1	0	0	Q_n (LS)	No change
1	0	1	0	Reset
1	1	0	1	set
1	1	1	$\overline{Q_n}$	Taggle

working:

Case I: J=K=0

with both inputs at logic 0 $S_1=0$, $R_1=0$ o/p of master FF remains in last state on positive edge of clock.

Case II: J=0, K=1

The high input K=1 goes to R_1 and low output goes to S_1. Due to high output from R_1 clock forces slave to reset. Hence flip-flop is in reset state.

Case III: J=1, K=0

The high input J=1 goes to S_1 and low input K=0 goes to R_1. Due to high output from S_1 clock forces slave to set. Hence flip-flop is in reset set.

case III: J=1, K=1

When J=1 and K=1 the output taggles on the positive transition of the clock and the slave taggles on the negative transition of the clock.

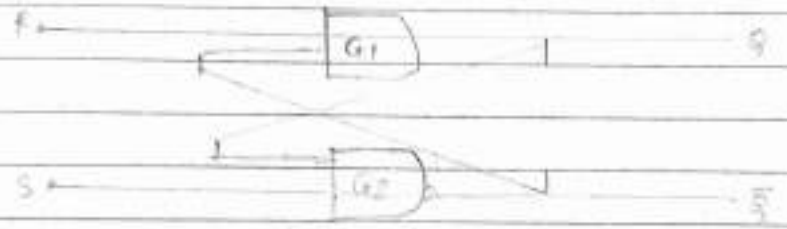
In the case of J-K flip-flop when J=1, K=1 the o/p taggles between 0 & 1 as the clock remains high under such conditions o/p is unpredictable this condition is called as race around condition This is drawback of J-K flip-flop

This can be avoided by:
i] Increasing the propagation delay time more than the clock pluse width.
ii] Triggering the flip-flop on clock edges.
iii] Isolating I/P & o/P of J-K flip-flop.

Q.2 short answer question:

- i] Explain working of RS Latch using NOR/NAND gates.

a] R-S Flip-flop using Nand Gate:



- RS Flip-Flop using NAND Gates consists of two NAND gates G_1 & G_2 in which output one is given to the I/P of other.

In case of NAND gate if one of the I/P is low the o/P is high.

Truth Table:

R	S	Q	action
0	0	forbidden	Race
0	1	1	set
1	0	0	Reset
1	1	LS	No change

working :

Case I : when $R = 0$, $S = 0$
with the $R = 0$ & $S = 0$ the output G_1 & G_2 goes high. i.e. $Q = \bar{Q} = 1$ but this is not allowed because Q & $\bar{Q}$ are always complementory. This state is called as forbidden state.

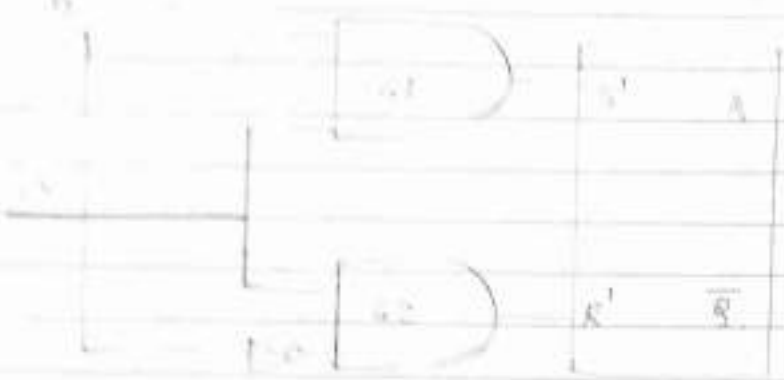
Case II : when $R = 0$, $S = 1$
with $R = 0$ the output of NAND gate G_1 becomes $Q = 1$, $S = 1$, the output of NAND gate G_2 $\bar{Q} = 0$ this condition is called as setting the flip-flop.

Case III : when $R = 1$, $S = 0$
with $R = 1$, $S = 0$ the output of NAND gate G_2, $\bar{Q} = 1$ as Q and $\bar{Q}$ are always complementary $Q = 0$
This is called as resetting the flip-flop

case IV : when $R = 1$, $S = 1$
with the both input high the flip-flop does not change it state because 1 I/P at the input of NAND gate has no effect on the output thus o/p remains in the last stage.

Suppose last stage is $Q = 1$ & $\bar{Q} = 0$ & I/P's to the NAND gate are $R = 1$, $S = 1$ then the output remains unchanged.

iii) Explain working of D-Flip-Flop with suitable diagram.



Logic diagram

A D Flip-Flop or D latch is level clocked. It consist of R-S flip-flop, two AND gates & a Not gate.

Truth Table

CLK	D	Q_{n+1}	Action
0	x	Last state	No change
1	0	0	Reset
1	1	1	set

Working:

In case of AND gate if one of the input is low output is low.

Case I: When clk is low (0):

When clock (CLK) is low both AND gates are disabled so D is in Don't care condition (x). i.e. 0 or 1

∴ O/P is in last state

∴ $Q_{n+1} = Q_n$

Case II: When CLK is high o/p depends upon the data I/P 'D'.

a] D = 0

When D = 0 upper AND gate provides low output & lower AND gate provides high output.

i.e. S = 0, R = 1 therefore o/p is in low state

$\therefore Q_{n+1} = 0$

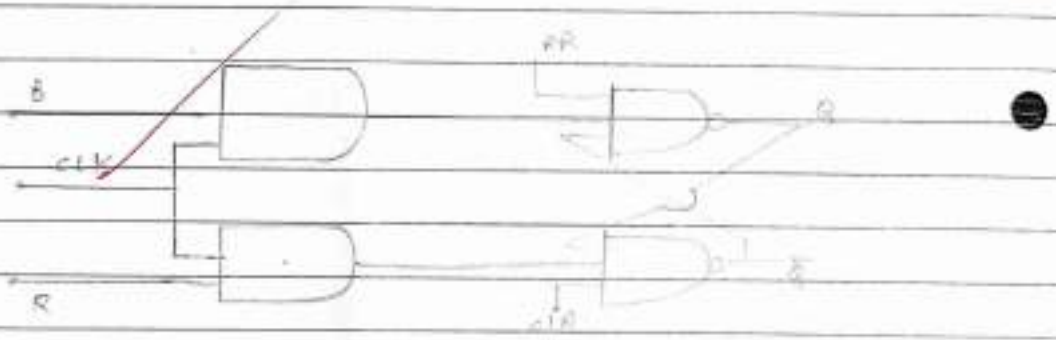
b] D = 1

When D = 1 upper AND gate provide high output & lower AND gate provide low output i.e. S = 1, R = 0 therefore o/p is high (1)

$\therefore Q_{n+1} = 1$

In D Flip-Flop the output follows the value D.

iii] Explain Present and clear concept with RS flip-flop



Present and clear concept facility of RS-FF:

In RS flip-flop OR gates provides present and clear inputs. upper OR gate provides PRESET & lower OR gate provides CLR I/P

OR gate provides high output if any one of I/P is high

case I : PR = 0, CLR = 1

When CLR = 1, lower OR gate passes reset signal.

$\therefore$ o/p $Q_{n+1} = 0$

Here CLR, R & S are don't care condition.

Truth Table:

PR	CLR	CLK	R	S	Q_{n+1}	Action
0	1	X	X	X	1	set
1	0	X	X	X	0	Reset
1	1	0	X	X	Q_n (LS)	No change
1	1	1	0	0	Q_n (LS)	No change
1	1	1	0	1	1	
1	1	1	1	0	0	
1	1	1	1	1	forbidden	

In case of NAND gate if one of the I/P is low O/P is high

Working

Case I : When PR=0 CLR=1

When PR=0 , CLR=1 lower OR gate passes reset signal

∴ output Q_{n+1} =0 here CLR

case II: When PR=1 , & CLR=0

When PR=1 CLR=0 upper OR gate passes set signal

∴output Q_{n+1} =1

Here CLK R, S are don't care condition.

caseIII: When PR=0 CLR=0 & CLK=1

The action is similar to normal clocked RS flip-flop

Case III: When PR=0 CLR=0 CLK=0

output remains in the last state R & S in don't care condition

PR=1 & CLR=1 not allowed it cause race condition.

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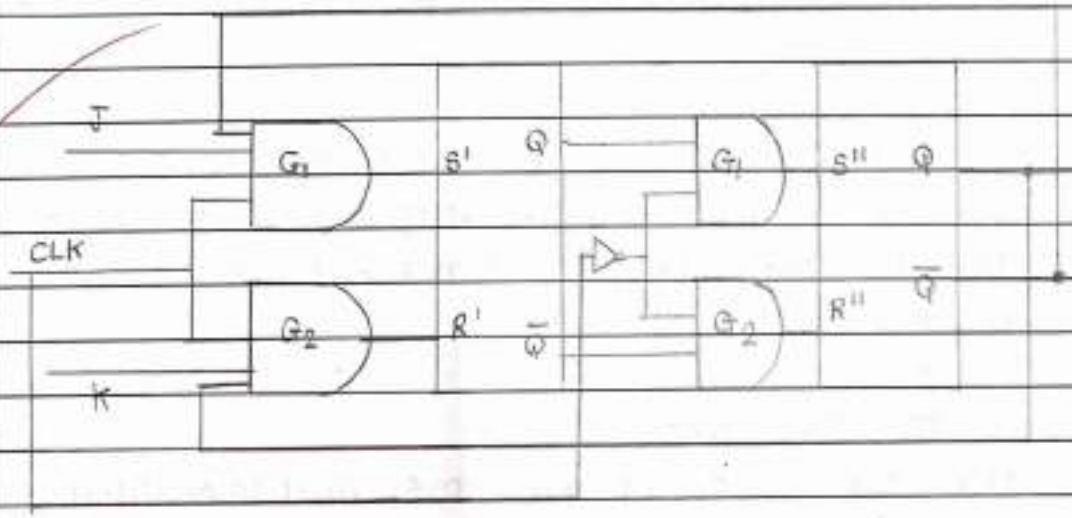
Name: Anushka Sunil Shete
Div : A , class - BSc-FY
Roll NO : 7318

Assignment

Q1. Long answer questions:

i] Explain the Master-slave JK Flip-Flop with proper logic diagram. How it overcome the race condition of J-K Flip-Flop.

→



08

J-K master slave flip-flop consists of two J-K flip-flops first is called the master which is positive edge triggred & second is called the slave which is negative edge triggered.

master flip-flop responds to I/P's J & K I/P's when clock is positive edge triggred. Slave flip-flop responds to the J & K when it is negative edge triggered.

Truth table:

CLK	J	K	Q_{n+1}	Action
0	X	X	Q_n (LS)	No change
1	0	0	Q_n (LS)	No change
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	$\overline{Q_n}$	Toggle

Working:

Case I : J = K = 0

With both inputs at logic 0 $S_1 = 0$, $R_1 = 0$ O/P of master FF remains in last state on positive edge of clock.

Case II : J = 0, K = 1

The high input K = 1 goes to R_1 and low output goes to S_1. Due to high output from R_1 clock forces slave to resest. Hence flip-flop is in reset state.

Case III : J = 1, K = 0

The high input J = 1 goes to S_1 and low input K = 0 goes to R_1. Due to high output from S_1 clock forces slave to set. Hence flip-flop is in reset state.

Case IV : J = 1, K = 1

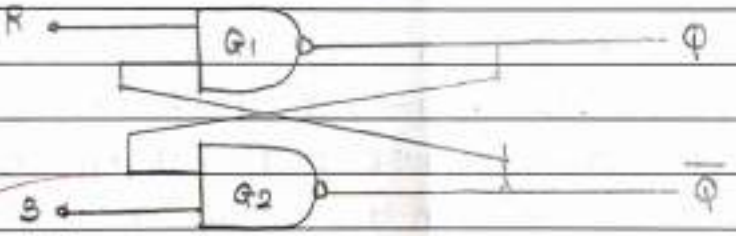
When J = 1 and K = 1 the output toggles between 0 & 1 on the positive transition of the clock and the slave toggles on the negative transition of the clock.

In case of J-K Flip-flop when J=1, K=1 the o/p toggles between 0 & 1 as the clock remains high under such condition o/p is unpredictable this condition is called as race around condition. This is drawback of J-K Flip-Flop
This can be avoided by :
i] Increasing the propagation delay time more than the clock pluse width.
ii] Triggering the flip-flop on clock edges.
iii] Isolating I/P & O/P of J-K Flip-flop

Q2. Short answer questions :

i] Explain working of RS latch using NOR/NAND gates.

a] R-S Flip-Flop using NAND Gate :



RS Flip-Flop using NAND Gates consists of two NAND gates G_1 & G_2 in which output one is given to the I/P of other.

In case of NAND gate if one of the I/P is low the o/p is high.

Truth Table :

R	S	Q	Action
0	0	Forbidden	Race
0	1	1	set
1	0	0	Reset
1	1	Is	No change

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working:

case I : when R=0, S=0
with the R=0 & S=0 the output G_1 & G_2 goes high. i.e $Q = \overline{Q} = 1$ but this is not allowed because Q & $\overline{Q}$ are always complementary. This state is called as forbidden state.

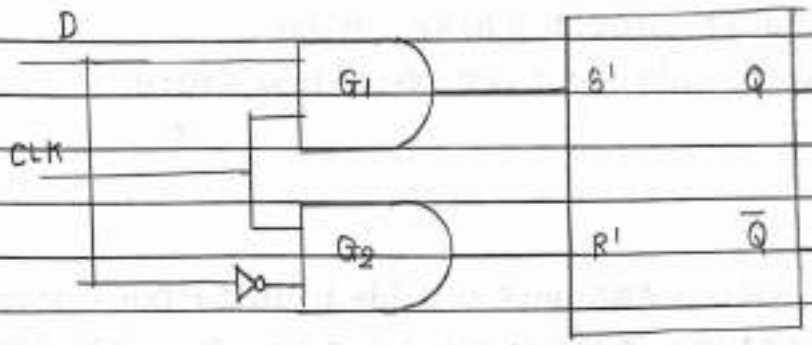
case II : when R=0, S=1
with R=0 the output of NAND gate G_1 becomes Q=1, S=1, the output of NAND gate G_2 $\overline{Q}$=0 this condition is called as setting the flip-flop.

case III : when R=1, S=0
with R=1, S=0 the output of NAND gate G_2, $\overline{Q}$=1 as Q and $\overline{Q}$ are always complementary Q=0. This is called as resetting the flip-flop.

case IV : when R=1, S=1
With the both the inputs high the flip-flop does not change its state because 1 I/p at the input of NAND has no effect on the output thus O/P remains in the last state.

Suppose last state is Q=1 & $\overline{Q}$=0, & I/P's to the NAND gate are R=1, S=1 then the output remains unchanged.

iii) Explain working of D flip-flop with suitable diagram.



Logic diagram

04 A D flip-flop or D latch is level clocked. It consist of R-S flip-flop, two AND Gates & a NOT Gate.

Truth table:

CLK	D	Q_{n+1}	Action
0	X	Last state	No change
1	0	0	Reset
1	1	1	Set

Working:

In case of AND gate if one of input in low output is low.

Case I: When CLK is low (0):

When clock (CLK) is low both AND gates are disabled so D is in Don't care condition (X). i.e 0 or 1

∴ O/P is in last state

∴ $Q_{n+1} = Q_n$

Case II: When CLK is high o/p depends upon the data I/P 'D'.

case II

a] D = 0

when D=0 upper & AND gate provides low output & lower AND gate provides high output.

i.e S=0, R=1 therefore o/p is in low state

$\therefore Q_{n+1} = 0$

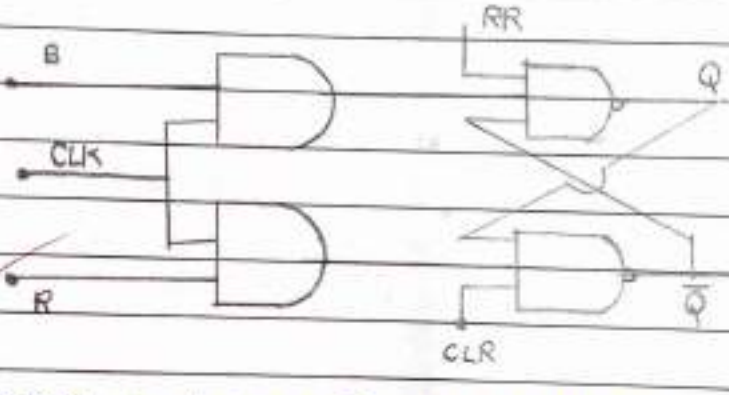
b] D = 1

when D=1 upper AND gate provide high output & lower AND gate provide low output i.e S=1, R=0 therefore O/P is high (1).

$\therefore Q_{n+1} = 1$

In D Flip-flop the output follows the value D.

iii] Explain Preset and Clear concept with Rs Flip-flop.



Preset and clear facility in Rs-ff:

In RS Flip Flop OR gates provides preset and clear inputs. upper OR gate provides PRESET & lower OR gate provides CLR I/P.

OR gate provides high output if any one of I/P is high.

Case I: PR=0, CLR=1

when CLR=1, lower OR gate passes reset signal. when

$\therefore$ O/P $Q_{n+1} = 0$.

Here CLR, R & S are don't care condition.

Truth table :

PR	CLR	CLK	R	S	Q_{n+1}	Action
0	1	X	X	X	1	Set
1	0	X	X	X	0	Reset
1	1	0	X	X	Q_n(LS)	No change
1	1	1	0	0	Q_n(LS)	No change
1	1	1	0	1	1	
1	1	1	1	0	0	
1	1	1	1	1	Forbidden	

In case of NAND gate if one of the I/P is low o/P is high.

Working :

CaseI : when PR = 0, CLR = 1
when PR = 0, CLR = 1, lower OR gate passes reset signal.
∴ output Q_{n+1} = 0 here CLR

CaseII : When PR = 1, & CLR = 0
when PR = 1, CLR = 0 upper OR gate passes set signal
∴ output Q_{n+1} = 1
Here CLK, R, S are don't care condition.

CaseIII : When PR = 0, CLR = 0 & CLK = 1
The action is similar to normal clocked RS-flip-flop.

Case IV : When PR = 0, CLR = 0, CLK = 0
output remains in the last state R & S in don't care condition.
PR = 1, & CLR = 1 not allowed it causes race condition.