"Dissemination of education through Knowledge, Science and Culture"
-Shikshanmaharshi Dr. Bapuji Salunkhe

Shri Swami Vivekanand Shikshan Sanstha's
VIVEKANAND COLLEGE, KOLHAPUR
(AUTONOMOUS)

Department of Electronics

Date: 06/04/2023

Notice

(B.Sc.I Electronics)

All the students of B.Sc.I Electronics are hereby informed that they should write a **Home assignment on Unit 2-Unipolar Devices of total 30 marks** on a full scape paper and submit to the department on or before 18/4/2023.

Q.1 Select correct alternative: [each for 1 mark] [2 marks]

1. A JFET is a..... driven device.

   (i) current (ii) voltage

   (iii) both current and voltage (iv) none of these

2. The input control parameter of a JFET is .....

   (i) gate voltage (ii) source voltage

   (iii) drain voltage (iv) gate current

Q.2 Long answer questions: [each for 8 marks] [16 marks]

i) Explain the N-channel JFET working, drain characteristics and transfer characteristics.

ii) Give the construction and working of D-MOSFET. Also draw its drain characteristic and explain it.

Q.3 Short answer questions: [each for 4 marks] [12 marks]

i. Explain the equivalent circuit of UJT.
ii. Explain the parameters of JFET.
iii. Draw and explain the characteristic of UJT.

VIVEKANAND COLLEGE ESTD. JUNE 1964 KOLHAPUR-416 003

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VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

B.Sc . - I 2022-23

Analog Electronics

Assignment-II :Unit -II: Unipolar Devices

Sr. No.	Roll No.	Student Name	Assignment Submitted	Marks
1	7201	AWATI SHREYASH DILIP	Not Submitted	0
2	7204	KAMBLE SAURABH SANJAY	Not Submitted	0
3	7207	LOKHANDE SUJAL SANDIP	Not Submitted	0
4	7208	MANGAONKAR VEDANT PRASHANT	Submitted	30
5	7209	MISAL OMKAR SUNIL	Submitted	29
6	7210	MUJAWAR ZAHIR JAMIR	Not Submitted	0
7	7211	NESARKAR SIDDHARTH DEEPAK	Submitted	18
8	7214	PATIL HARSHAD RAJGONDA	Not Submitted	0
9	7219	SHELAKE RUPALI	Not Submitted	0
9	7215	PATIL HARSHVARDHAN DHANANJAY	Not Submitted	0
10	7223	WARANGE NIRAJ RAJESH	Submitted	30
11	7224	YADAV HARSH NIVAS	Not Submitted	0
12	7229	BHADARAGE ABHISHEK SUNIL	Submitted	28
13	7279	ALANBAGI AHMED QASIM HASAN	Not Submitted	0
14	7281	ASANEKAR YASH TUKARAM	Submitted	26
15	7282	BAMANE SAHIL NIVRUTI	Submitted	29
16	7283	BAVACHE SHRAVANI BHIMRAV	Submitted	22
17	7284	CHOUGULE SAI CHANDRAKANT	Submitted	28
18	7285	CHOUGULE VAIBHAVI JAYSING	Submitted	21
19	7286	DHUMALE SANIKA SANTOSH	Submitted	30
20	7287	GHUMAI DHIRAJ BABASO	Submitted	29
21	7288	GURAV SANIKA RAVINDRA	Submitted	24
22	7289	HIRDEKAR SHREYA SHASHIKANT	Submitted	30
23	7291	KANGRALKAR GAYATRI GUNDU	Submitted	29
24	7292	KUMBHAR DIKSHA YUVRAJ	Submitted	30
25	7293	KUMBHAR PRATHMESH YUVRAJ	Submitted	30
26	7294	KUMBHAR SANIKA SANJAY	Submitted	29
27	7296	MANE AARATI PRAKASH	Submitted	23
28	7297	MANE ADITYA SHARAD	Submitted	29
29	7299	NANAVARE ADARSH VIJAY	Submitted	21
30	7301	NIMBALKAR SAIRAJ NANDKUMAR	Submitted	24
31	7302	PARPOLKAR SANIKA SUBHASH	Submitted	19
32	7303	PATIL ADITYA MANSING	Not Submitted	0
33	7304	PATIL KIRTI SAMBHAJI	Submitted	30
34	7305	PATIL POONAM NARSU	Submitted	30
35	7306	PATIL PRADNYA PRADIP	Submitted	28
36	7307	PATIL PRATHAMESH BHAGAVAN	Submitted	28
37	7308	PATIL RAVIRAJ BAJIRAO	Not Submitted	0

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38	7309	PATIL RIYA NITIN	Submitted	30
39	7310	PATIL SAHIL VISHNU	Submitted	21
40	7311	PATIL SAMARTH SHRIKANT	Submitted	17
41	7312	PATIL SAMMED DHANYAKUMAR	Not Submitted	0
42	7313	PATIL SOURABH BHAGAWAN	Submitted	12
43	7314	PHADAKE SUMIT RAMBHAU	Not Submitted	0
44	7317	SAWANT PRATHAM PRADEEP	Submitted	29
45	7318	SHETE ANUSHKA SUNIL	Submitted	30
46	7319	SURVE VIKRANT RAJENDRA	Submitted	19
47	7320	TIWADE KETAN GIRISHKUMAR	Submitted	29
48	7325	GHODE VAISHNAVI SHRIKANT	Submitted	30
49	7332	LAMBE SANKET JAYKUMAR	Submitted	18
50	7333	LOLAGE GAYATRI GAJANAN	Submitted	30
51	7344	PATIL SHARVARI KULDEEP	Submitted	29
52	7550	DADDIKAR GAURAV NITIN	Not Submitted	0
53	7551	ALTEKAR ADITYA MAHESH	Submitted	29
54	7563	AHMED SAMI ALITTIBIN	Submitted	21
55	7567	PATIL SWAPNIL SURESH	Submitted	28
56	7569	SHINDE RUGVED TANAJI	Not Submitted	0
57	7584	PATIL PRATHMESH KALLAPPA	Not Submitted	0

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30/30

Riya Nitin Patil
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Assignment

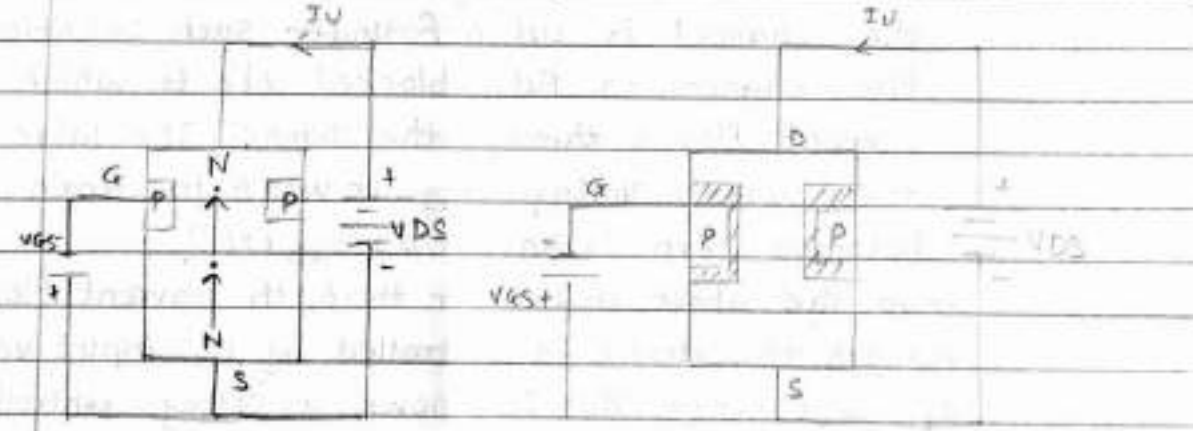
Q.1

1. A JFET is a voltage driven device.

2. The input control parameter of a JFET is gate voltage.

Q.2

i] Explain the N-channel JFET working, drain characteristics and transfer characteristics.



Bias voltage for operation of n-channel JFET

Above figure shows the circuit for n-channel JFET with normal polarities i.e. gate is reverse biased The drain is made positive w.r.t source so that drain current I_D flows from the source so that drain. The circuit operation takes place as follows:

Sulekha

1] When voltage V_D is applied between drain and source and if $V_{GS} = 0$, then the two pn-junctions at the side of the bar establish depletion layers. The electrons flow from source to drain through a channel between the depletion layers. The size of these layer determine the width of the channel and hence the current conduction through the bar.

2] When the reverse voltage V_{GS} is applied between the gate and source the width of depletion layer is increased. This reduces the width of the channel and hence current flow through the channels. reduce on the other hand if reverse voltage on the gate is decreased, the width of the depletion layer also decreases result in the increase in width of the conducting channel. Hence the current flowing through the channel increases.

3] If the reverse voltage V_{GS} on the gate is continuosuly increased, a state is reached when the two depletion layers touch each other and the channel is cut off. Under such conditions, the channel is fully blocked due to which no current flows through the channel. The value of these reverse voltage V_{GS} at which the drain current becomes zero is known as V_{GS} (off)

from the above it is clear that, the current flowing through the device is controlled by the input voltage V_{GS} and hence this is known as voltage controlled device or field Effect Transistor.

The following fig. represents the drain characteristic of n-channel JFET.

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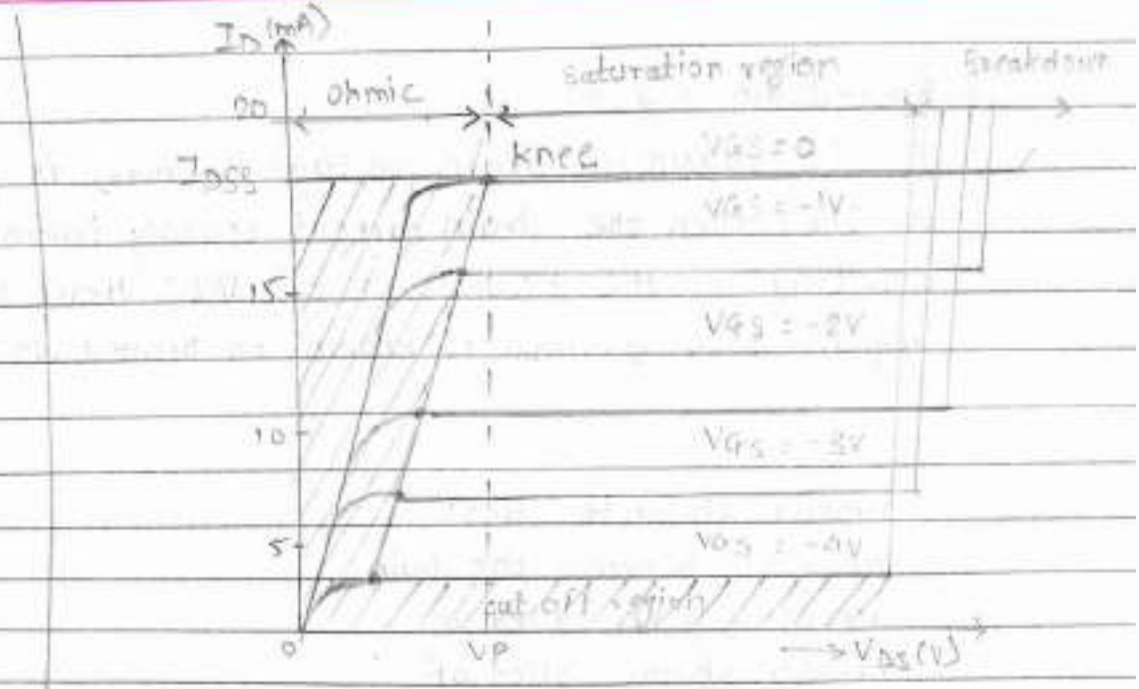


1. Ohmic region:

IF the gate is shorted with source, the maximum drain current flows through the channel which is denoted as I_{DSS} and known as shorted gate drain current. This region is shown as curve as in fig. In this region the drain current ID increases linearly with the increase in drain to source voltage V_{DS} obeying ohm's law. This linear characteristic is due to the fact that n-type semiconductor bar acts like a simple resistor.

2. Curve AB (saturation region):

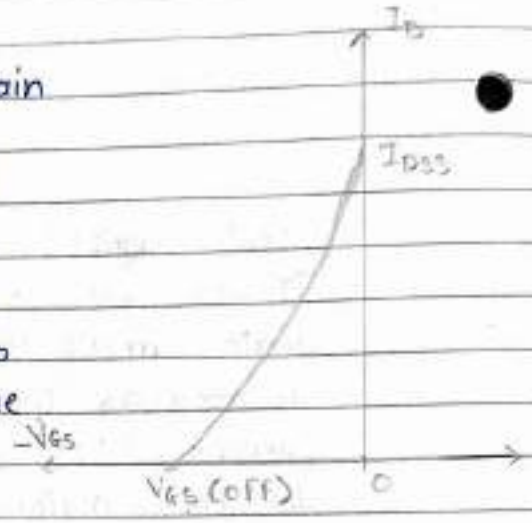
At point A the drain current almost becomes constant; After pinch off voltage channel the width becomes so narrow that the depletion layer almost touch each other. The drain current is passed through the small passage between these layer and hence increase in drain current is very small with V_{DS} above pinch off voltage V_P. Where I_D is constant is known as active region, where JFET works as a constant current source.

3. Breakdown region:

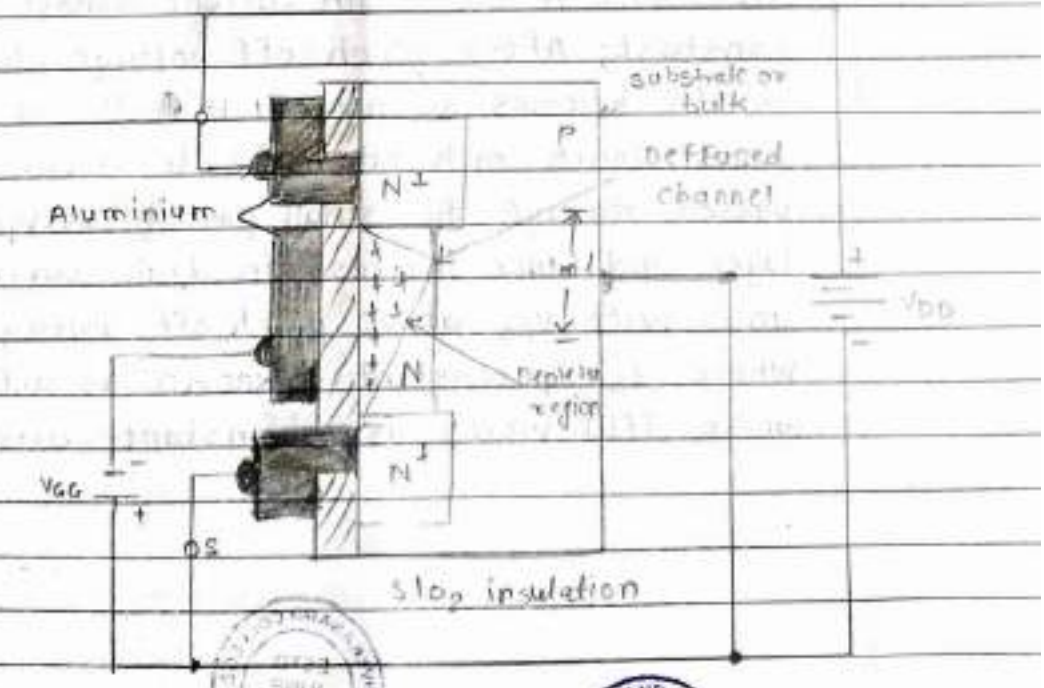
If the maximum drain voltage $V_{DS(max)}$ is applied to JFET then the drain current sharply increases resulting in the breakdown of JFET. Hence the region above $V_{DS(max)}$ is known as breakdown region.

Transfer characteristics:

The graph between the drain current I_D & V_{GS} called as transfer characteristics of FET from the graph it is clear that I_D is maximum when $V_{GS} = 0$ and I_D is zero for maximum reverse value of V_{GS}. The JFET must be operated below $V_{GS(off)}$



ii] Given the construction and working of D-MOSFET Also draw its drain characteristic and explain it.



The above diagrams show the constructional details of n-channel D-MOSFET

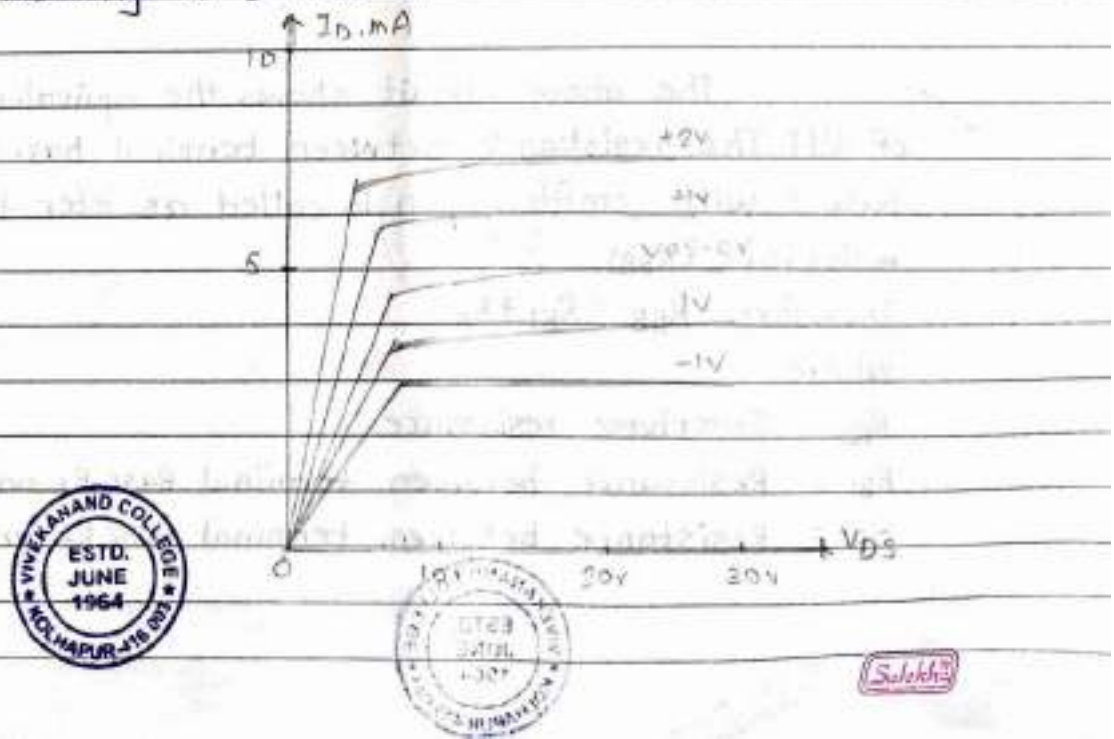
i] The n-channel D-MOSFET is a piece of n-type material diffused in a p-type region (called substrate) and an insulated gate on the left as shown in fig. The free electrons flowing from source to drain must pass through the narrow channel between the gate and the p-type region. (i.e substrate)

ii] During gate construction a thin layer of metal oxide (usually silicon dioxide, SiO_2) is deposited over a small portion of the channel. A metalic gate is deposite over the oxide layer. As SiO_2 is an insulator, therefore gate is insulated from the channel. The arrangment forms a capacitor. one plate of these capacitor is the gate and the other plate is the channel with SiO_2 as the dielectric.

iii] Since the gate is insulated from the channel, the MOSFET is sometimes called insulated gate FET (IGFET)

iv] It is a usual practice to connect the substrate to the source (S) internally so that a MOSFET has three terminals viz source (S), gate (G) and drain (D).

Working of D-MOSFET:

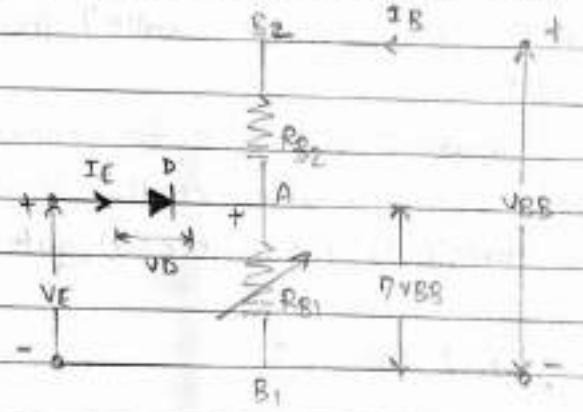


i] When $V_{GS} = 0V$, a significant current flows for a given V_{DS}.

ii] When the gate is made negative, the other plate the channel has a positive charge included in it opposite the gate. This serves to deplete the channel of majority carries (electrons) so the conductivity decreases, giving rise to characteristic curves like the JFET.

iii] When the gate is mde positive, the otherplate, the channel has negative charge induced in it opposite gate. so the conductivity increases and enhancing current flow as shown in fig.

i] Explain the equivalent circuit of UJT.



The above circuit shows the equivalent circuit of UJT. The resistance between terminal base 1 and base 2 with emitter open is called as inter-base resistance (R_{BB})

Therefore $R_{BB} = R_{B1} + R_{B2}$

where

R_{BB} = Interbase resistance

R_{B1} = Resistance between terminal Base B_1 and emitter.

R_{B2} = Resistance between terminal Base B_2 and emitter.

The value of interbase resistance lies is in the range of 4.7kΩ to 10kΩ. The value of R_{B1} and R_{B2} is depend upon where the P type material is located along the n type bar material.
As the emitter (E) is located closer to base 2 terminal, the resistance R_{B2} is greater than the resistance R_{B1}.
The battery R_{BB} is connected between terminal B base 1. and Base 2 as shown in fig.
The point A acts as voltage divider point for resistance R_{BB}.
Let the voltage drop across resistance R_{B1} is V_A.
According to voltage divider rule,

$$V_A = \left[\frac{R_{B1}}{(R_{B1}+R_{B2})}\right] V_{BB}$$

$$V_A = \eta V_{BB}$$

The η is called as intrinstic stand off ration and its value lies in range of 0.5 to 0.85
∴ The intrinsic standoff ratio is given by,

$$\eta = \left[\frac{R_{B1}}{(R_{B1}+R_{B2})}\right]$$

ii] Explain the parameter of JFET.

The parameter of JFET is as follow:

a] ac drain resistance (rd):

It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate-source voltage i.e.

$$\text{a.c drain resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}$$

For instance, if a change in drain voltage of 2V produces a change in drain current of 0.02 mA then,

$$\text{a.c drain resistance, } rd = \frac{2V}{0.02mA} = 100K\Omega$$

b] Transconductance (g_{fs}):

The control that the gate voltage has over the drain current is measured by transconductance g_{fs}

It may be defined as follows:

It is the ratio of change in drain current (ΔI_D) to the change in gate-source voltage (ΔV_{GS}) to constant drain-source voltage i.e.

4

$$\text{Transconductance, } g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}$$

The transconductance of a JFET is usually expressed either in mA/Volt or micromho. As ex. if a change in gate voltage of 0.1V causes change in drain current of 0.3 mA then,

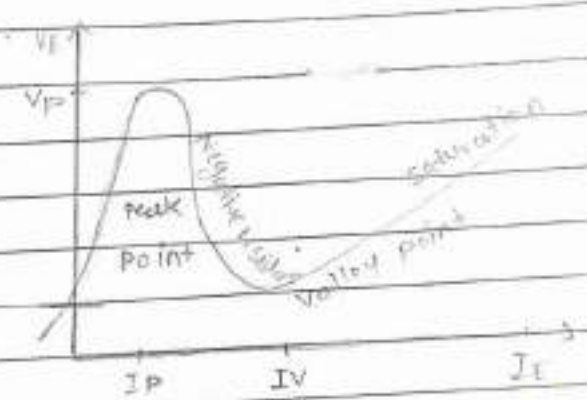
$$\text{Transconductance, } g_{fs} = \frac{0.3\,mA}{0.1V}$$

$= 3mA/V = 3\times10^{-3}$ A/V or mho or S (siemens)

$= 3\times10^{-3}\times10^{6}\,\mu$mho $= 3000\,\mu$mho (or μS)

iii] Draw and explain characteristics of UJT.

→ A unijunction transistor is a three terminal semiconductor device having only one p-n junction like diode but has three terminals. The device has a unique characteristic that when it is triggered, the emmiter current increases regenarative until is limited by emitter power supply. The unijunction transistor can be employed in a variety of applications like switching pulse generator, s awtooth generator etc.



4 The basic construction of UJT and its symbol is shown in above fig. It consists of an N-type silicon bar with an electrical connection on each end and the leads to these connections are called base leads, Base 1 (B_1), Base 2 (B_2). The small p-type region is doped at one side of the bar near to B_2 terminal and that lead taken from this type p-junction is known as emitter region. Thus a p-n junction is formed.

Total reverse biased $V_p + V_B = V_D + \eta V_{BB}$

i.e. $V_p = \eta_{BB} + V_D$

30/30

Gayatri Gajanan Lolage
Roll No - 7933
Div - A BSC-I

Assignment

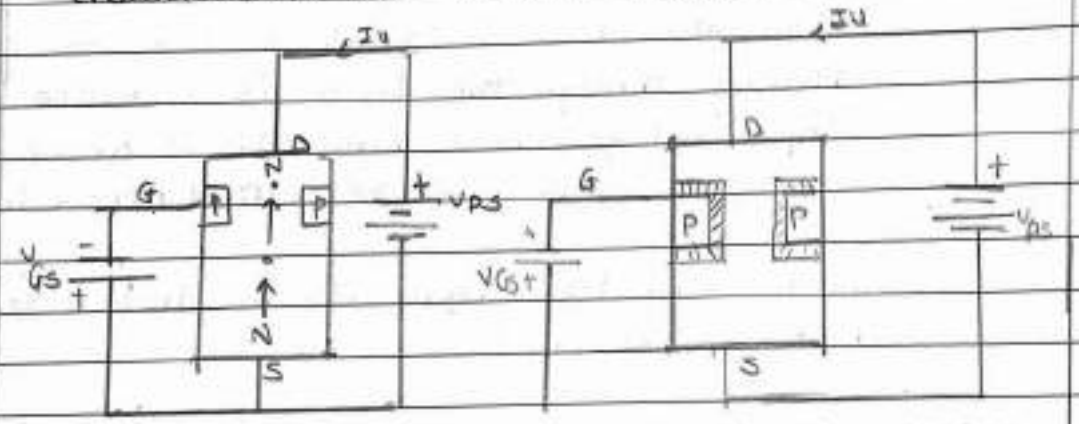
Q1.

1. A JFET is a voltage driven device

2. The input control parameter of a JFET is gate voltage

Q2.

i) Explain the N-channel JFET working, drain characteristics and transfer characteristics.



Bias voltage for operation of n-channel JFET

Above figure shows the circuit for n-channel JFET with normal polarities i.e gate is reverse biased The drain is made positive w.r.t. source so that drain current I_D flows from the source to drain The circuit operation takes place as follows:

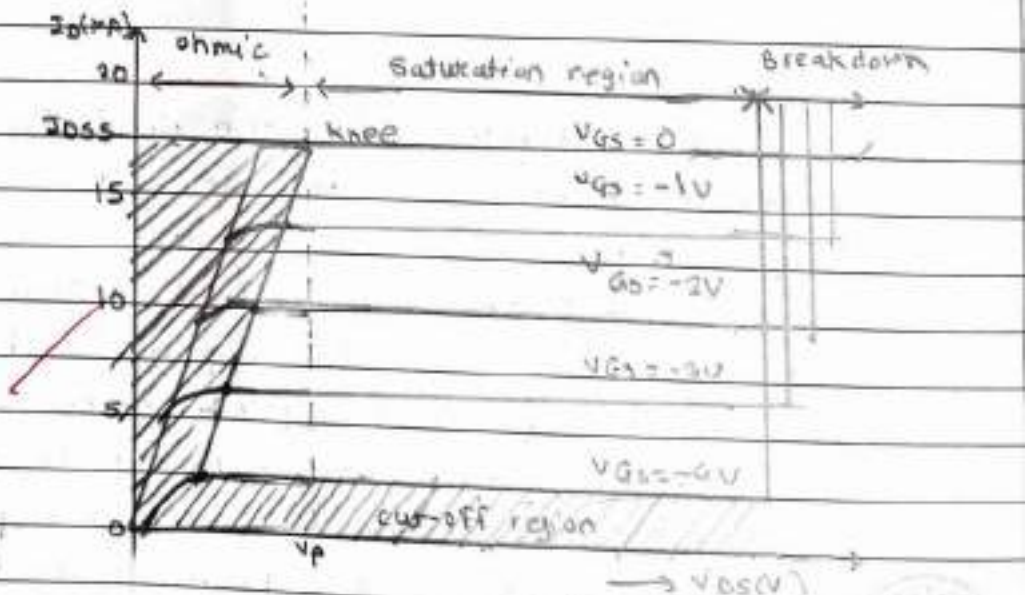
1) when voltage V_D is applied between drain & Source and if $V_{GS} = 0$, then the two pn-Junctions at the sides of the bar establish depletion layers The electrons will flow from source to drain through a channel between the depletion layers The size of these layers determines the width of the channel and hence current conduction through the bar.

2] When the reverse voltage V_{GS} is applied between the gate and source the width of depletion layer is increased. This reduces the width of the channel and hence current flowing through the channel reduces. On the other hand if reverse voltage on layer also decreased, resulting in the increases in width of the conducting the channel. Hence the current flowing through the channel increases.

3] If the reverse voltage V_{GS} on the gate is continuously increased, a state is reached when the two depletion layer touch each other and the channel is cut off. Under such conditions, the channel is fully blocked due to which of this reverse voltage V_{GS} at which the drain current becomes zero is known as $V_{GS(OFF)}$.

From the above it is clear that, the current flowing through the device is controlled by the input voltage V_{GS} & hence this is known as Voltage controlled device or Field Effect Transistor.

The following figure represents the drain characteristics of n-channel JFET.



1 ohmic region.

If the gate is shorted with source, the maximum drain current flows through the channel which is denoted as I_{DSS} and know as Shorted gate drain current. This region is shown as curve OA in figure. In this region the drain to source V_{DS} obeying Ohm's law. This linear characteristic is due to the fact that the n-type semiconductor bar acts like a simple resistor.

2. Curve AB (saturation region)

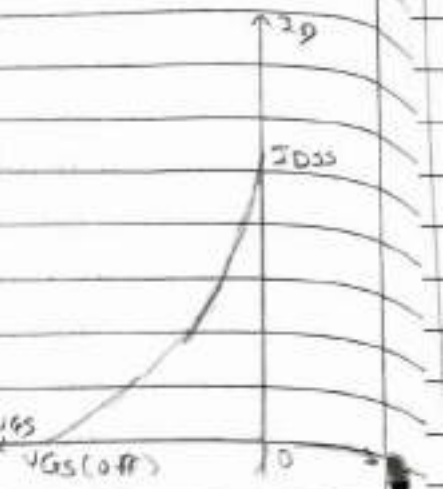
At point A the drain current almost become constant this value of V_{DS} above which the I_D becomes constant is called as pinch off voltage V_p. After pinch off voltage the channel width becomes so narrow that the depletion layer almost touch each other. The drain current is passed through the small passage between these layers and hence increase in drain current is very small with V_{DS} above pinch off voltage V_p. Consequently drain current I_D remains constant. This region where I_D is constant is known as active region, where JFET works as a constant current source.

3. Breakdown region:

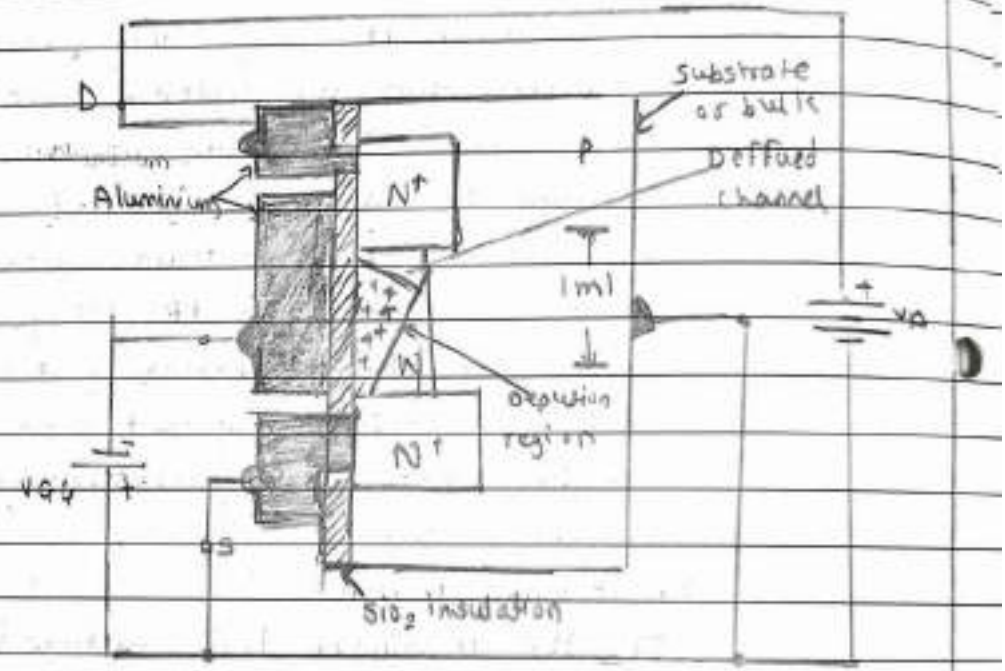
If the maximum drain voltage $V_{DS(max)}$ is applied to JFET then the drain current sharply increases resulting in the breakdown of JFET. Hence the region above $V_{DS(max)}$ is known as breakdown region. Hence the voltage applied to drain should be less than $V_{DS(max)}$ for safty purpose.

Transfer characteristic:

The graph between the drain current I_D and V_{GS} called as transfer characteristics of FET. from the graph it is clear that I_D is maximum when $V_{GS} = 0$ & I_D is zero for maximum reverse value of V_{GS}. The JFET must be operated below $V_{GS(OFF)}$



i] Give the construction and working of D-MOSFET also draw its drain characteristic & explain it



The above diagram shows the constructional details of n-channel D-MOSFET.

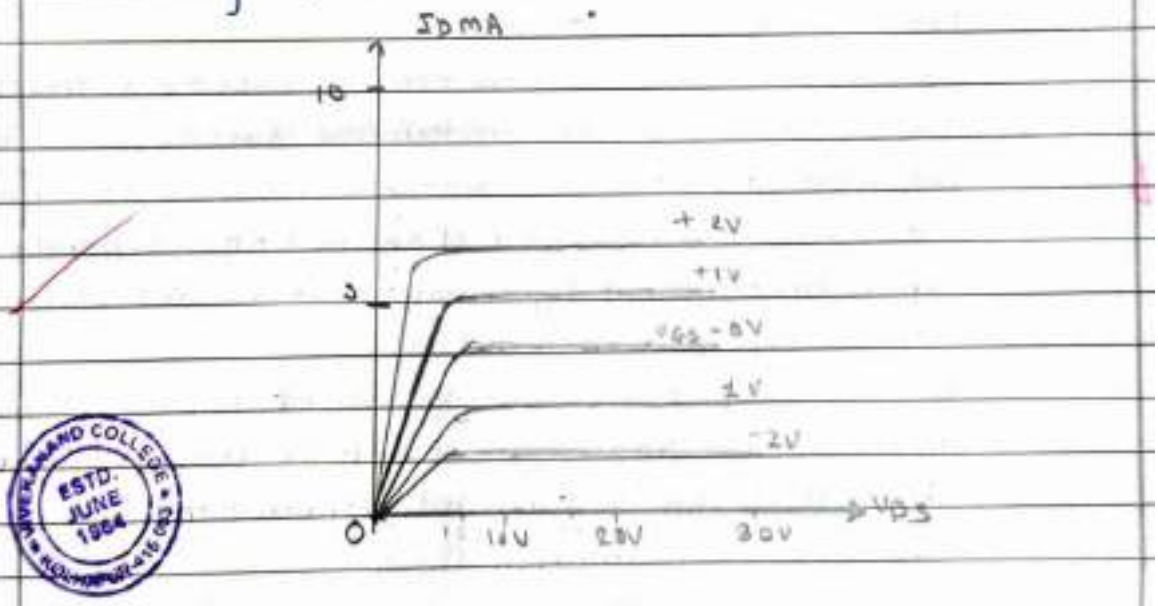
i] The n-channel D-MOSFET is a piece of n-type material diffused in a p-type region (called substrate) and an insulated gate on the left as shown in fig. The free electrons flowing from source to drain must pass through the narrow channel between the gate and the p-type region. (i.e substrate)

ii) During gate construction a thin layer of metal oxide (usually silicon dioxide, SiO_2) is deposited over a small portion of the channel. A metalic gate is deposited over the oxide layer As SiO_2 is an insulator therfore, gate is insulated from the channel. The arrangement forms a capacitor one plate of this capacitor is the gate and the other plate is the channel with SiO_2 as the dielectric

iii) Since the gate is insulated from the channel, the MOSFET is sometimes called insulated-gate FET (IGFET)

iv) it is a usual practice to connect the substrate to the source(s) internally so that a MOSFET has three terminals viz source(s), gate(G) & drain(D)

Working of D-MOSFET:

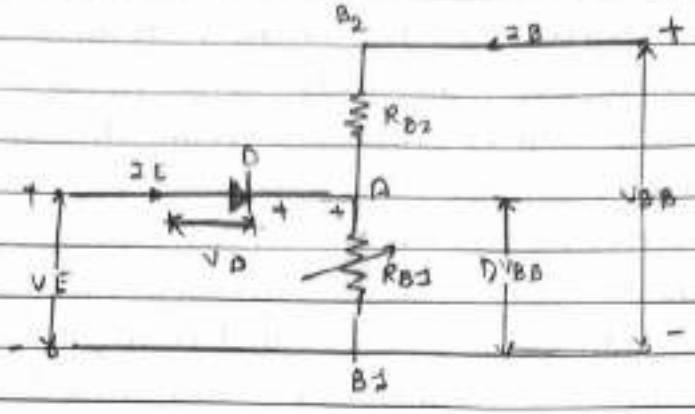


i) when $V_{GS} = 0V$, a significant current flows for a given V_{DS}

ii) when the gate is made negative, the other plate the channel has a +ve positive charge induced in it opposite the gate. This serves to deplete the channel of majority carriers (electrons) so the conductivity decreases, giving rise to characteristic curves like the JFET

iii) when the gate is made positive, the other plate the channel has negative charge induced in it opposite the gate, This serves to enhance the channel of majority carriers so conductivity increases & enhancing current flows as

1] Explain the equivalent circuit of UJT.



The above circuit shows the equivalent circuit of UJT. The resistance between terminal base 1 and base 2 with an emitter open is called as inter-base resistance (R_{BB})

Therefore $R_{BB} = R_{B1} + R_{B2}$

where,

R_{BB} = Interbase resistance

R_{B1} = Resistance between terminal Base B_1 & emitter

R_{B2} = Resistance between terminal Base B_2 & emitter

The value of interbase resistance lies is in the range of 4.7 KΩ to 10 KΩ. The value of R_{B1} and R_{B2} depends upon where the P type material is located along the n-type bar material.

As the emitter (E) is located closer to base 2 terminal, the resistance R_{B2} is greater than the resistance R_{B1}.

The battery V_{BB} is connected between terminal base 1 and base 2 as shown in figure.

The point A acts as voltage divider point for resistance R_{BB} let the voltage drop across resistance R_{B1} is V_A

According to voltage divider rule,

$$V_A = \left[\frac{R_{B1}}{(R_{B1} + R_{B2})} \right] V_{BB}$$

$$V_A = \eta V_{BB}$$

The η is called as intrinsic stand off ratio and its value lies in range of 0.9 to 0.86.
Therefore the intrinsic stand off ratio is given by

$$\eta = \left[\frac{R_{B1}}{(R_{B1}+R_{B2})} \right]$$

iii] Explain the parameters of JFET.

The parameters of JFET are as follows :

a] a.c drain resistance (rd) :

it is the ratio of change in drain - source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate - source voltage i.e.

$$\text{a.c drain resistance, } r_d = \frac{\Delta V_{DS} \text{ at constant } V_{GS}}{\Delta I_D}$$

for instance, if a change in drain voltage of 2V produce a change in drain current of 0.02 mA then

$$\text{acdrain resistance } r_d = \frac{2V}{0.02mA} = 100\ K\Omega$$

b] Transconductance (g_{FS}) :

The control that the gate voltage has over the drain current is measured by transconductance g_{FS}

It may be defined as follows

It is the ratio of change in drain current (ΔI_D) to the change in gate - source voltage (ΔV_{GS}) at constant drain - source voltage i.e.

$$\text{Transconductance, } g_{FS} = \frac{\Delta I_D \text{ at constant } V_{DS}}{\Delta V_{GS}}$$

The transconductance of a JFET is usually expressed either in mA/volt or micromho. As an example, if a change in gate voltage of 0.1V causes a change in drain current 0.3mA

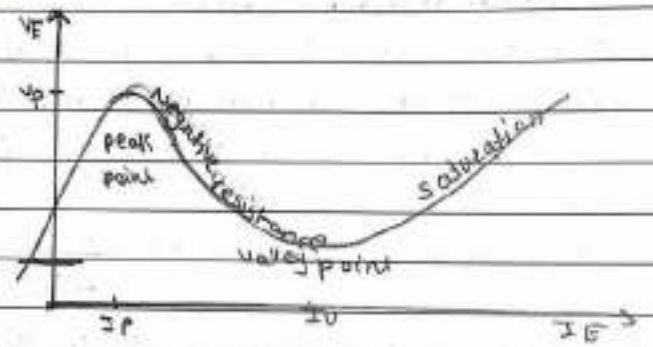
$$\text{Transconductance, } g_{FS} = \frac{0.3mA}{0.1V}$$

$= 3mA/V = 3\times10^{-3}$ A/V or mho or S (siemens)

$= 3\times10^{-3} \times 10^{6}\ \mu$ mho $= 3000\ \mu$ mho (or μS)

iii) Draw and explain characteristic of UJT.

→ A unijunction transistor is a three terminal semiconductor device having only one p-n junction like diode but has three terminals. The device has a unique characteristic that when it is triggered, the emitter current increases regenerative until is limited by emitter power supply. The unijunction transistor can be employed in a variety of applications like switching pulse generator, a sawtooth generator etc.



4 The basic construction of UJT and its symbol is shown in above fig. It consists of an N type silicon bar with an electrical connection on each end and the leads to these connections are called base lead B, Base 1 (B1), Base 2 (B2). The small P-type region is doped at one side of the bar near to B2 terminal & that lead taken from this p-type region is known as emitter region thus a p-n junction is formed.

Here emitter diode is reverse biased by voltage drop across resistance R_{B1} and its own barrier potential VD so total reverse bias is $V_{B1} + V_D = V_{B1} + \eta V_{BB}$. The value of emitter voltage which causes the diode conduction is called peakpoint Voltage Vp i.e. $V_p = \eta V_{BB} + V_D$.

Then, the UJT is turned on & emitter current begins to flow. under this condition the UJT is said to fired or triggered turned on.

Thus as V_E along with I_E increases R_{B1}, η & V_A decreases this produces further decreasg in R_{B1}, η and V_A. This process is regenerative V_A as well as V_E decreases as I_E increases. Due to this the UJT has negative resistance region in its V-I characteristics. the curve between emitter voltage V_E and emitter current I_E of a UJT at a given voltage V_{BB} between the bases, this is known as emitter characteristic of UJT.

18/30

Name:- Siddharth Deepak Nesarkar
Sub:- Electronics Batch:- E1
Roll No:- 7211 Div:- A Std:- BSC-I FY

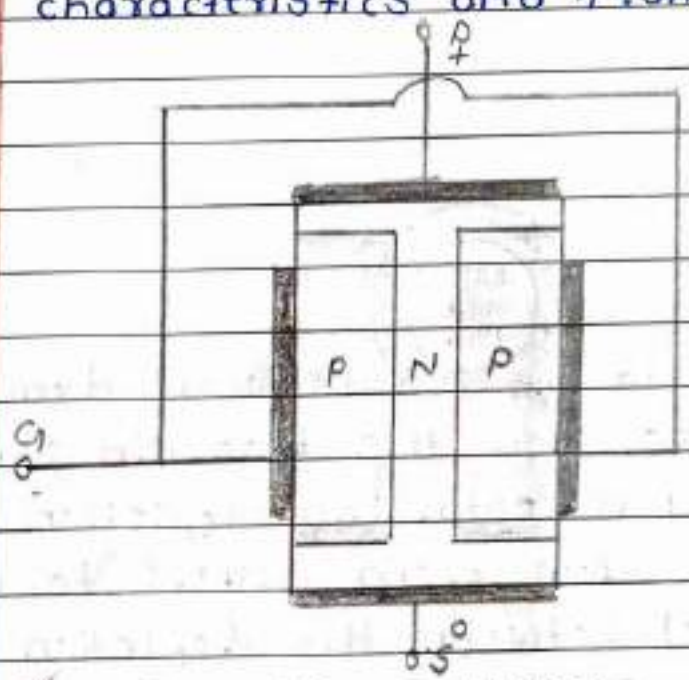
Q1. Select correct alternative.

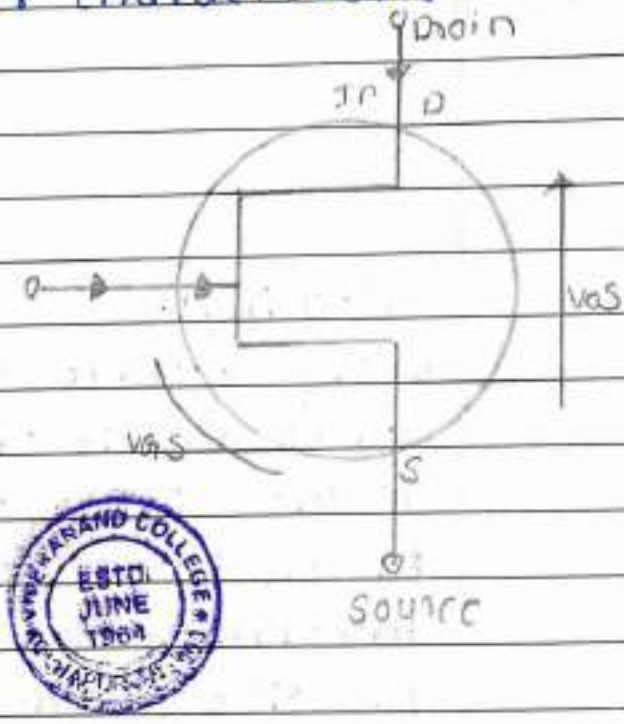
1) A JFET is a voltage driven

2) The input control parameter of a JFET is

Q2. Long answer question.

1) Explain the N-channel JFET working, drain characteristics and tranfer characteristic





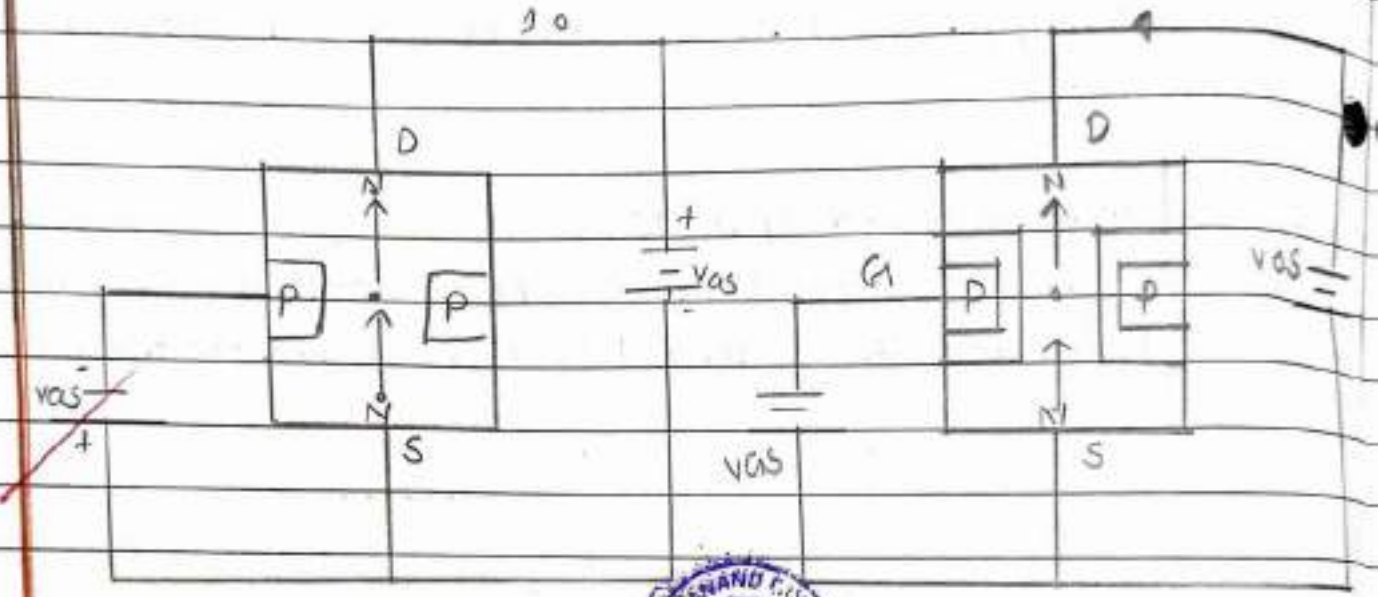
STRUCTURE OF N-JFET

1) A junction field effect transistor is a three terminal semiconductor devices in which current conduction is by an type of carrier i.e electrons and holes and it is controlled by means of an electric field between the gate electrode and the conducting channel of the device. The JFET

has high input inpedance and low noise level.

2] A JFET consists of a n-type silicon bar containing two pin junctions at the sides of the bar forms the conducting channel for the charge carriers. If the bar is n-type, it is called n-channel JFET.

Fig: Bias voltage for operation of n-channel JFET



Working:-

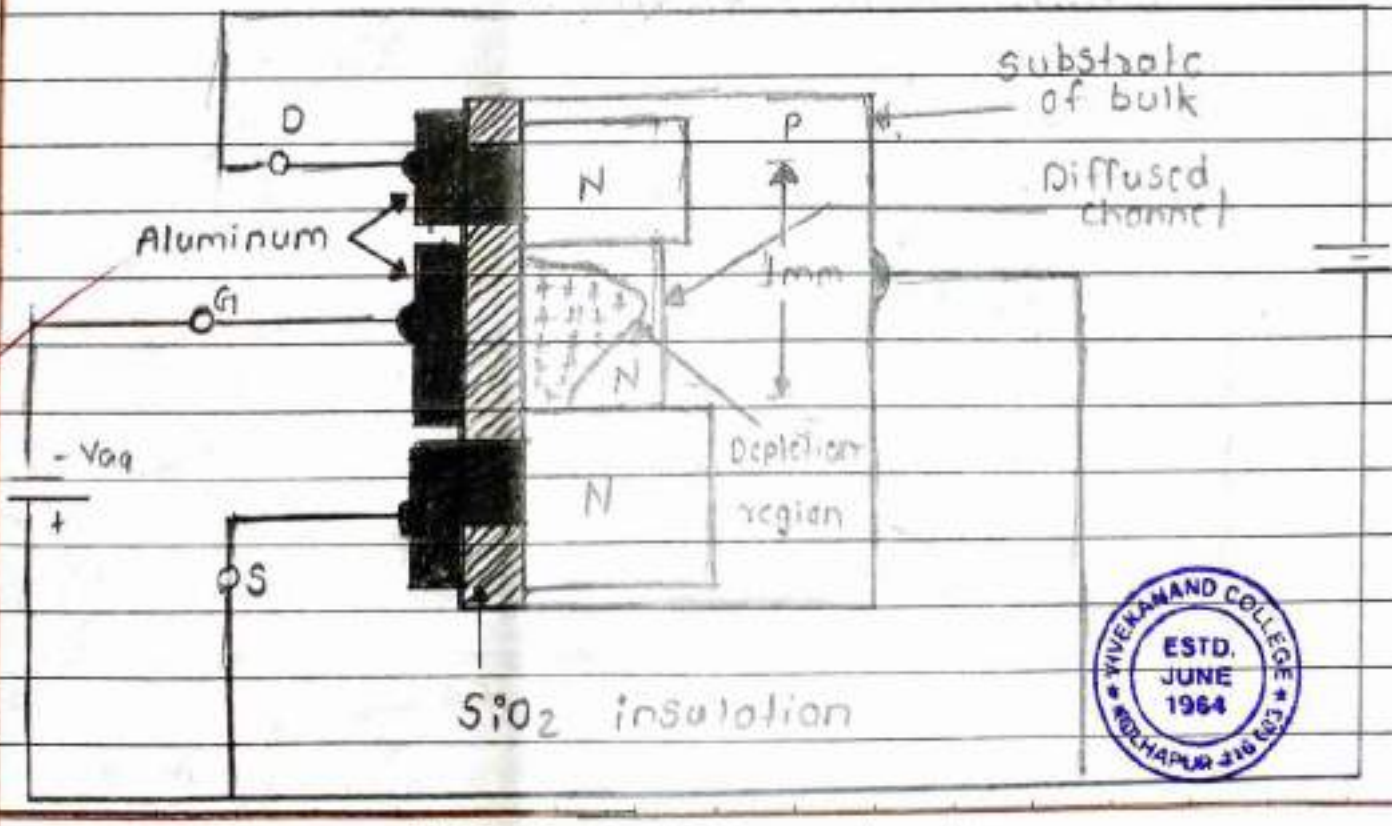
1] When voltage VDS is applied between drain and source and if VGS = 0, then the two p/n junctions at the sides of bar establish depletion layers. The electrons will flow from source to drain through a channel between the depletion layers. The size of these layers determines the width of the channel and hence the current conducti through the bar.

2] When the reverse voltage VGS is applied between the gate and source, the width of the depletion layer is increased. This reduces the width of the channel and hence current

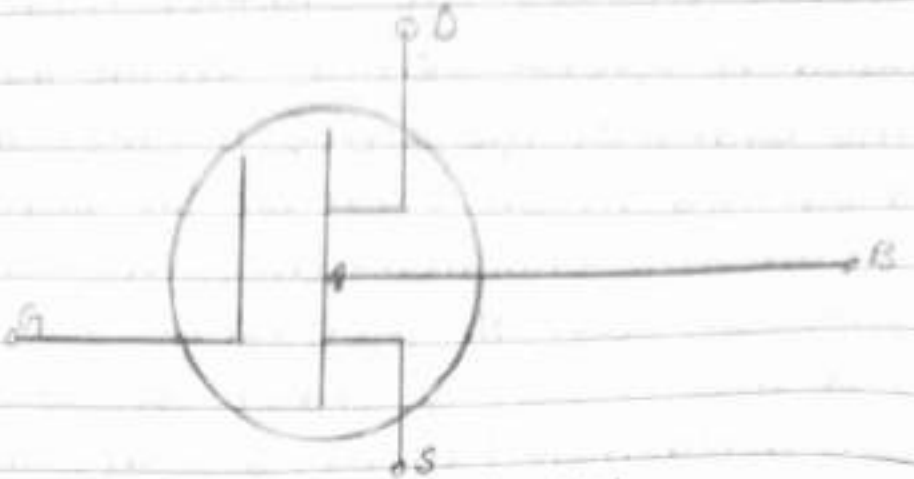
Flowing through the channel reduces. On the other hand if reverse voltage on the gate is decreased, the width of the depletion layer also decreases resulting in the increase in width of the conducting channel. Hence the current flowing through circuit increases.

3] If the reverse voltage V_{GS} on the gate is continuously increased, a state reached when the two depletion layers touch each other and the channel is cut off (pinched off) under such conditions, the channel is fully blocked due to which no current flows through the channel. The value of this reverse voltage V_{GS} of which the drain current becomes zero is known as $V_{GS(OFF)}$.

1] Give the Construction and working of D-MOSFET. Also draw is drain characteristic and explain it.



D-Type MOSFET Construction

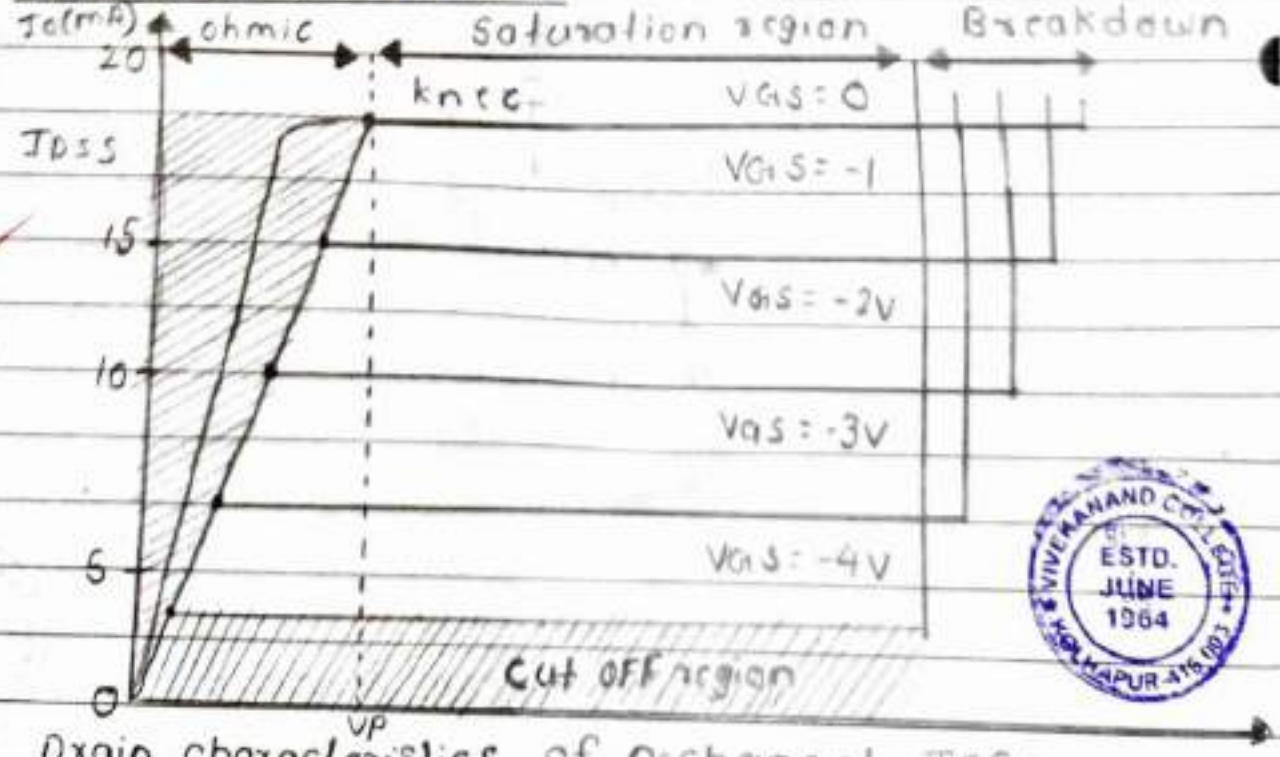


D TYPE MOSFET symbol.

Construction:-

1) The n-channel D-MOSFET is a piece of n-type material diffused in a P type region (called substrate) and an insulated gate on the left as shown in Fig. The free electrons flowing from source to drain must pass through the narrow channel between the gate and the P-type region (i.e substrate).

Drain characteristics:-

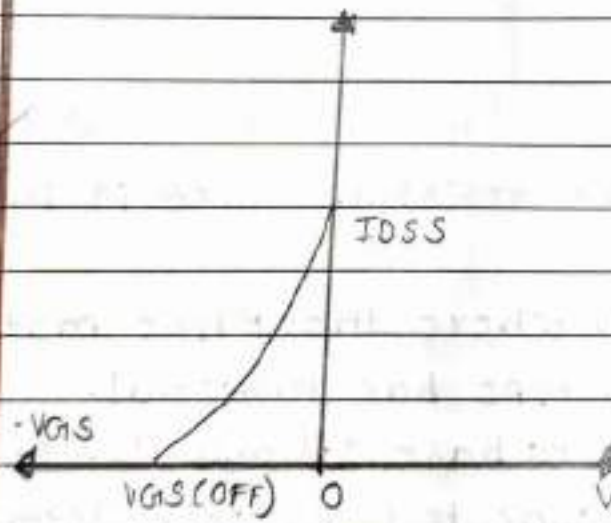


Drain characteristics of n-channel JFET

The output characteristics are shown, which can be difined as the graph between the output current Io and output voltage Vos keeping the input voltage VGS constant. The different curves for different values of VGS are shown in fig from the graph the following points can be noted in order to explain typical shape of output characteristics we select the curve with VGS=0 which is subdivided in the following regions.

1) ohmic region
2) Curve AB (saturation region)
3) Breakdown region.

Transfer characteristic: The graph between the drain current Io and VGS is called FET from the graph it is clear that Io is maximum when VGS=0 and Io is zero for maximum reverse value of VGS. The JFET must be operated below VGS (OFF).



Q3. Short answer questions.

1) Explain the equivalent circuit of UJT.

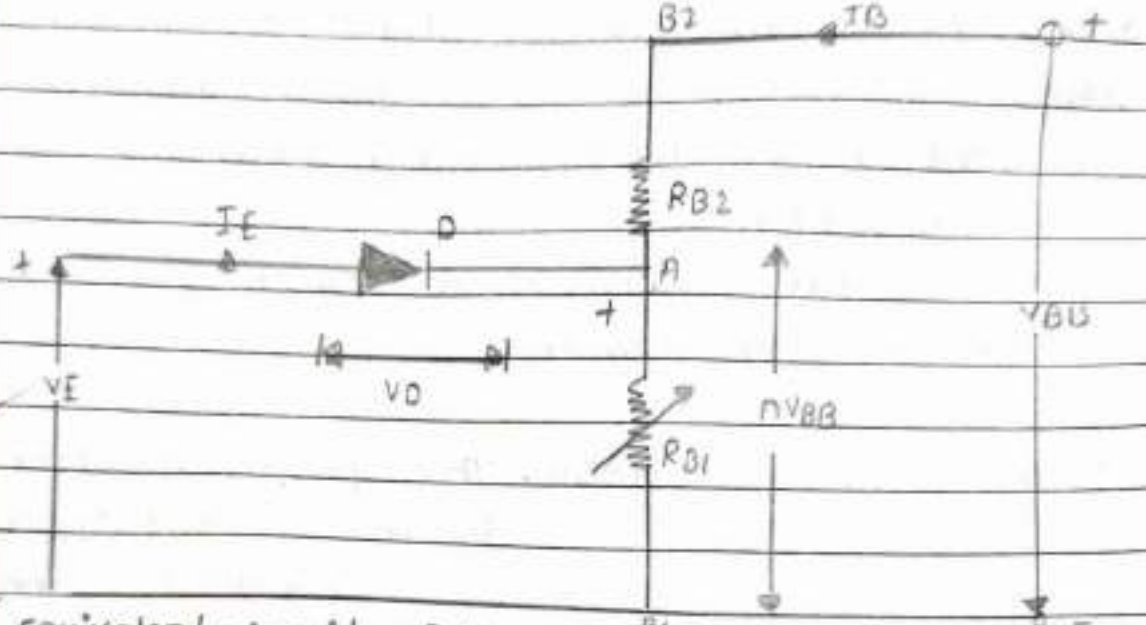
→ The equivalent circuit of the UJT is shown in Fig. below the resistance between terminal base 1 and base 2 with emitter open is called as inter-base resistance (RBB).

$\therefore R_{BB} = R_{B1} + R_{B2}$

where, R_{B1} = Resistance between terminal Base B_1 and emitter.

R_{B2} = Resistance between terminal Base B_2 and emitter.

R_{BB} = Interbase resistance.



Equivalent circuit of the UJT intrinsic standoff ratio (η)

1) The value of interbase resistance lies is in the range 4.7 - 10kΩ.

2) R_{B1}, R_{B2} depends upon where the P type material is located along then n-type bar material.

3) Emitter (E) is closer to base 2 terminal $\therefore R_{B2} > R_{B1}$

4) The battery V_{BB} is connected between terminal B_1 and B_2 as shown in Fig.

ii] During gate construction a thin layer of metal oxide is deposited over a small portion of a channel. A metallic gate is deposited over the oxide layer. As SiO_2 is an insulator, therefore, gate is insulated from the channel. Note that the arrangement from a capacitor. one plate of this capacitor is the gate and other plate is the channel with SiO_2 as the dielectric.

iii] Since the gate is insulated from the channel, the mosfet is sometimes called insulated gate FET (IGFET).

iv] It is usual pratice to connect the substrate to the source (S) internally so that a MOSFET has three terminals that is source (S), gate (G) & drain (D)

v] Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. Therefore D-MOSFET can be operated in both depletion mode and enhancement mode.

Drain characteristics for a depletion type of MOSFET

Page No.
Date

Working of D-MOSFET:

1) When $V_{GS}=0V$, a significant current flows for a given V_{DS}.
2) When the gate is made negative the other plate, the channel has a positive charge induced in it opposite the gate. This serves to deplete the channel of majority carriers (electrons) So the conductivity decreases giving rise to characteristic curves like the JFET.
3) When the gate is made positive, the other plate the channel has negative charge induced in it opposite the gate. This serves to enchance the chanel of majority charge carriers. So the conductivity increases and enchancing current flows.
4) The point A acts as voltage dividers point for the resistance R_{BB}.
5) Let the voltage drop across resistance R_{B1} is V_A According voltage dividers rule.

$$V_A = \left[\frac{R_{B1}}{(R_{B1}+R_{B2})}\right] V_{BB}$$

$$V_A = \eta V_{BB}$$

6) The η is called as inhrinsic stand off ratio and its value lies in the range of 0.5 and 0.85.

$$\eta = \left[\frac{R_{B1}}{(R_{B1}+R_{B2})}\right]$$

2] Explain the parameters of JFET.

→ i) AC drain resistance (rd): It is the ratio of change in drain-Source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate Source voltage.

AC drain resistance,

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$ at constant V_{GS} rd value varies from 10KΩ to 1MΩ.

ii) Transconductance (g_{fs}):

The control that the gate voltage has over the drain current is measured by transconductance g_{fs} It is the ratio of change in drain current (ΔI_D) to the change in gate Source voltage (ΔV_{GS}) at constant drain Source voltage.

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$$ at constant V_{DS} the transconductance is usually expressed either in mA/volt or micromho.

iii) Amplification factor (μ):

It is the ratio of change in drain Source voltage (ΔV_{DS}) to the change in gate-Source voltage (ΔV_{GS}) at constant drain current i.e

Amplification factor $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$ of constant I_D

'μ' indicates how much more control the gate voltage has over drain current than has the drain voltage.

3] Draw and explain characteristics of UJT.

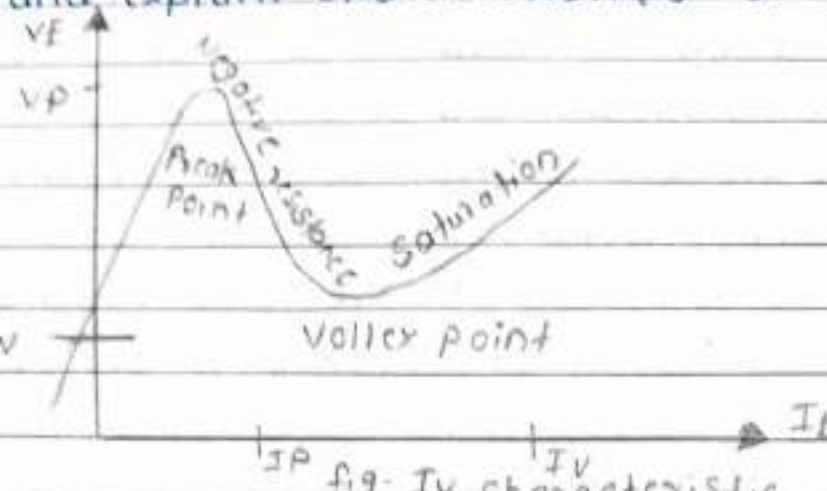


fig. Iv characteristic

1] The curve between emitter voltage VE and emitter I of a UJT at a given voltage VBB between the bases, this is known emitter characteristics of UJT.

2] Initially in the cut off region, as VE increases from zero, slight leakage current flows from terminal B2 to the emitter. the current is due to the minority carriers in the reverse biased diode.

3] Above a certain value of VE forward current IE begin to flow, increasing until the peak voltage Vp and current Ip are reached at point P.

4] After the peak point P an attempt to increase V is followed by sudden increase in emitter current IE with decrease in VE is a negative resistance Portion of the curve.

5] The negative resistance portion of the curve lasts until the valley point Vp is reached with valley point voltage Vv and the valley point current Iv after valley point the device is driven to saturation. The difference Vp-VS is a measure of switching efficiency of UJT fall as VBB decreases.

21/30

Name - Patil Sahil Vishnu
Roll - 7310
Subject - electronics

Q.1 Select correct alternative

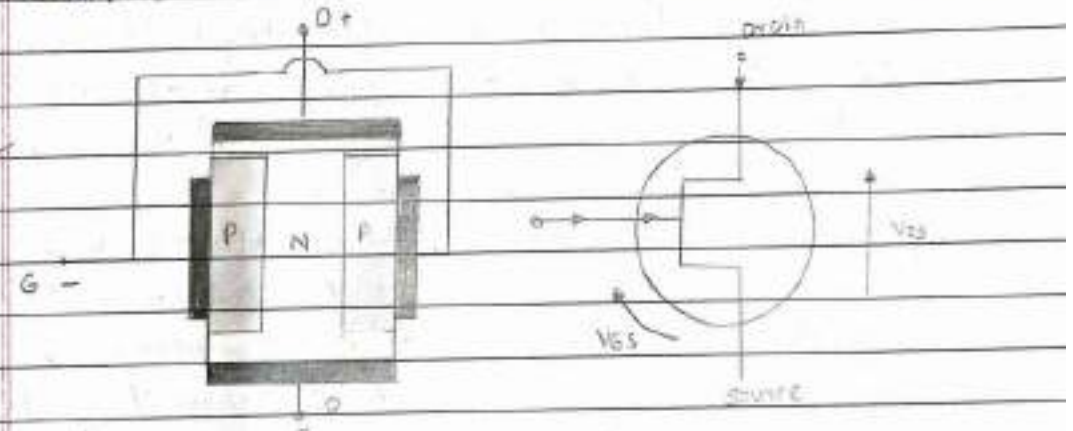
1. A JFET is a voltage driven

2. The input control parameter of a JFET is

Q.2 Long answer question.

i] Explain the N-channel JFET working, drain characteristics and transfer characteristic.

→



structure of N-FET

A Junction filed effect transistor is a three terminal semiconductor devices in which current conduction is by an eletric filed between the gate electrode and the conducting channel of the device. The JFET has high input impedance and low noise level.

A JFET consists of a n-type silicon bar containing two pin junctions at the sides. The bar forms the conducting channel for the charge carrics.

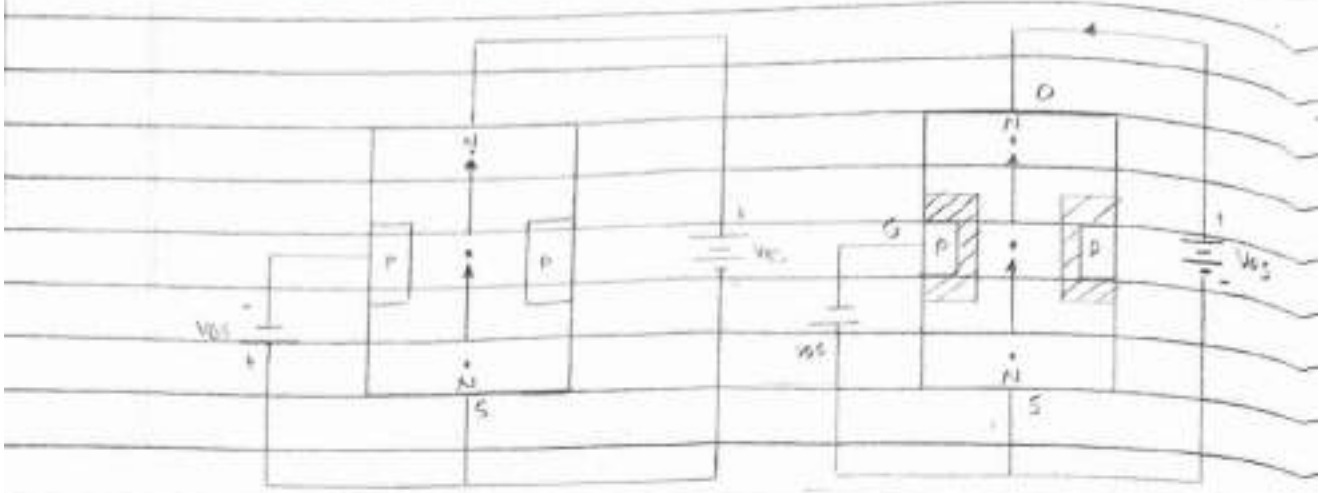


Fig:- Bias voltage for operation of n-channel JFET

working :-

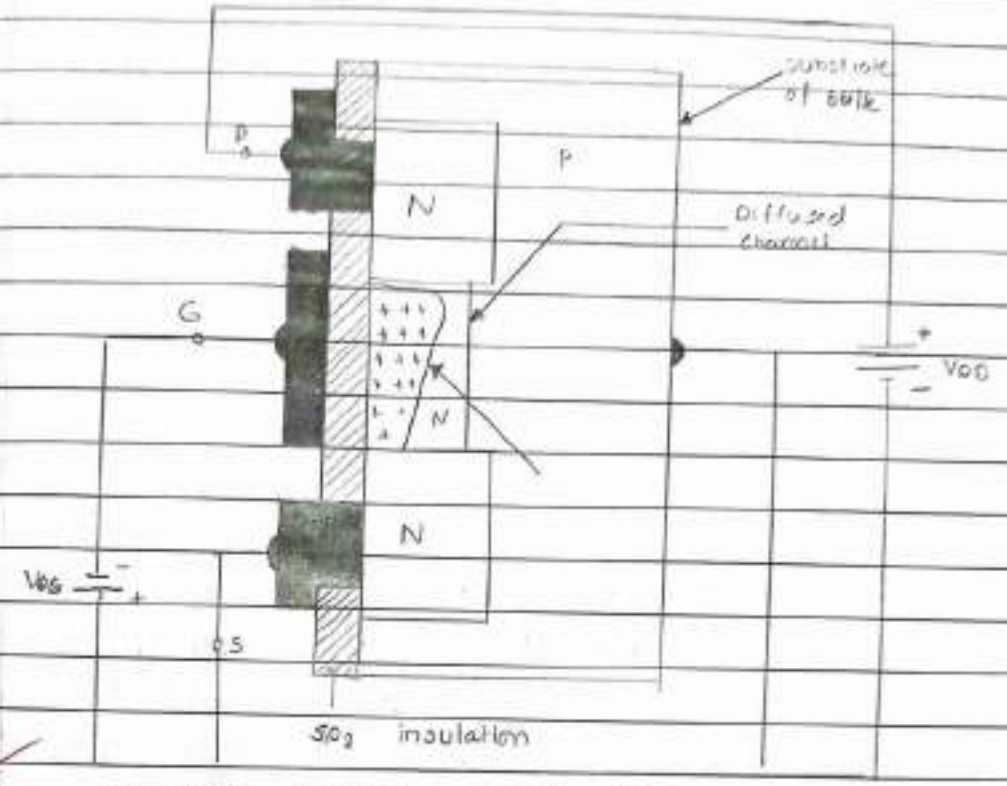
1] when voltage VDS is applied between drain and source and if VGS = 0, then the two PN junctions at the sides of bar establish depletion layers. the electron will flow from source to drain through a channel between the depletion layers. The size of these layers determines the width of the channel and the current conduction through the bar.

2] When the reverse voltage VGS is applied between the gate and source, the width of the depletion layer is increased. This reduce the width of the channel and hence current flowing through the channel reduces. on the other hand if reverse voltge on the the gate is decreased, the width of the depletion layer also decreased resulting in the increase in width of the conducting channel.

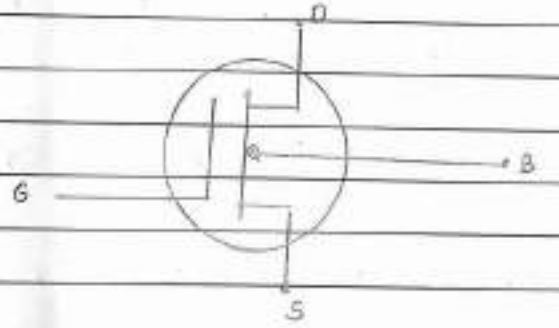
3] if the reverse voltage VGS on the gate is continously increased, a state reached when the two depletion layer touch each other and the channel is cut off (pinched off) under such conditions, the channel is fully blocked due to which the channel

ii] Give the construction and working of D-MOSFET. Also draw its drain characteristic and explain it.

→



D Type MOSFET construction

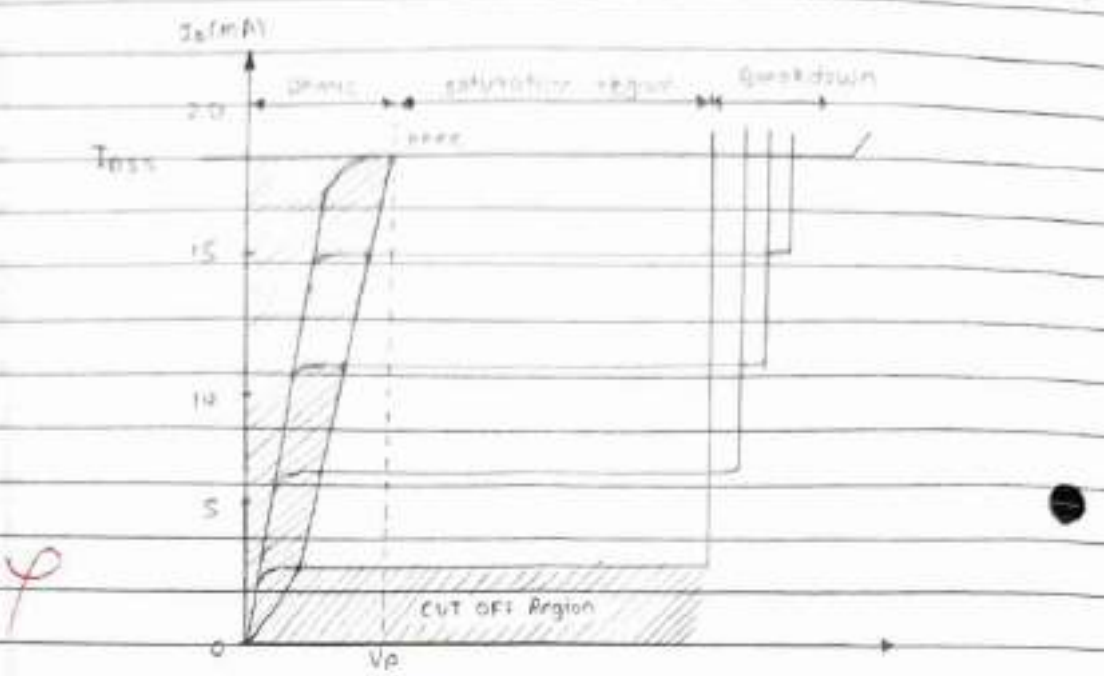


D Type MOSFET Symbol

Construction :-

1] The n-channel D-MOSFET is a piece of n-type material diffused in a p type region (called substrate) and an insulated gate on the left as shown in fig. the free electrons flowing from source to drain must pass through the narrow channel between the gate and the p-type region. (i.e. substrate)

Drain characteristics:

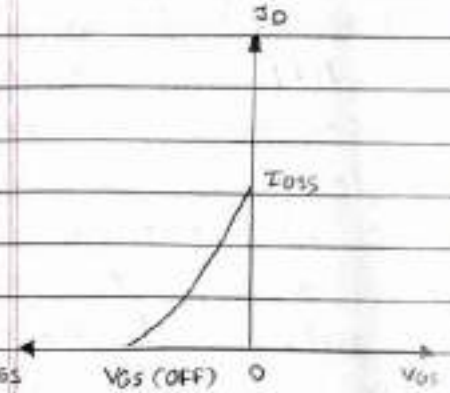


Drain characteristics of N-channel JFET

The output characteristics are shown, which can be defined as the graph between the output current I_D and output voltage V_{DS} keeping the input voltages V_{GS} constant. the different curves for different values of V_{GS} are shown in fig from the shape of output characteristics, we select the curves with $V_{GS} = 0$ which is subdivided in the following regions.

1) ohmic regions.
2) curve AB (Saturation region)
3) Breakdown region.

Transfer characteristic:- The graph between the drain current I_D and V_{GS} is called as transfer characteristics of FET. from the graph it is clear that I_D is maximum when $V_{GS} = 0$ and I_D is zero for maximum reverse value of V_{GS}. The JFET must be operated below $V_{GS(off)}$



Page No.
Date

Q.3 short answer questions

i] Explain the equivalent circuit of UJT.

→

The equivalent circuit of the UJT is shown in fig. below the resistance between terminal base 1 and base 2 with emitter open is called as inter-base resistance (R_{BB}).

$\therefore R_{BB} = R_{B1} + R_{B2}$

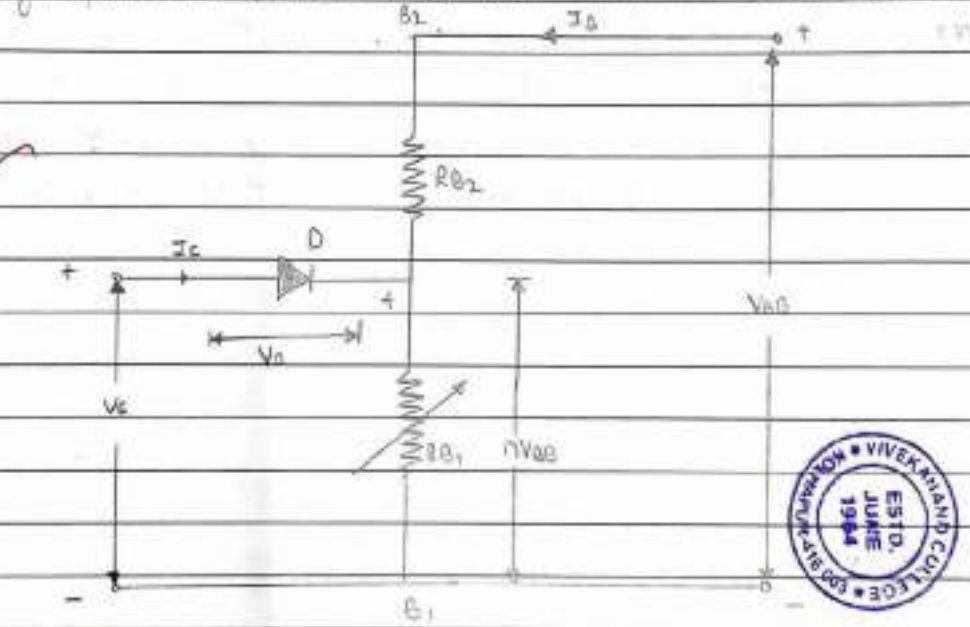
where,

R_{B1} = Resistance between terminal base B_1 and emitter.

R_{B2} = Resistance between terminal base B_2 and emitter.

R_{BB} = Inter base resistance.

Fig:- equivalent circuit of the UJT intrinsic standoff ratio



1] the value of inter base resistance lies is in the range 4.7 - 10 kΩ.

2] R_{B1}, R_{B2} depends upon where the p type material is located along the n-type bar material.

3] Emitter (E) is closer to base 2 terminal $\therefore R_{B2} >$

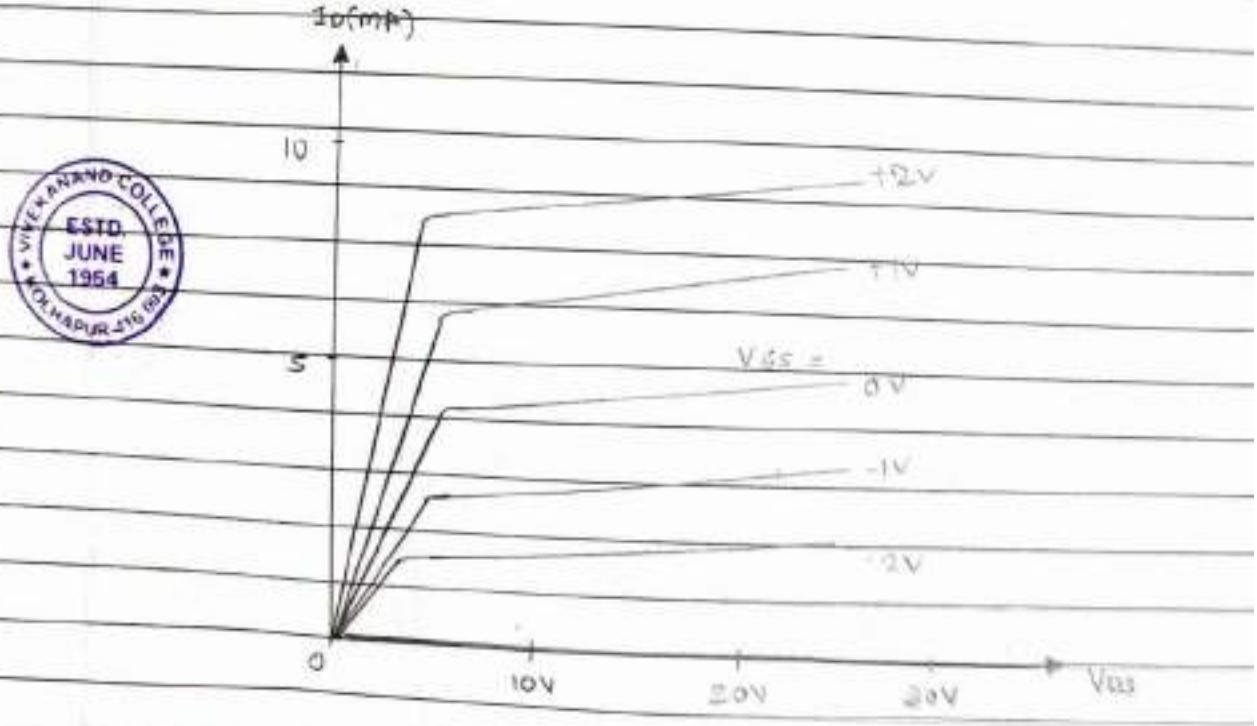
4] The battery V_{BB} is connected between terminal B_1 and B_2 as shown in fig.

ii] Using gate construction a thin layer of metal oxide is deposited over a small portion of a channel. A metallic gate is deposited over the oxide layer. As SiO_2 is an insulator, therefore, gate is insulated from the channel. Note that the arrangement forms a capacitor one plate of this capacitor is the gate and other plate is the channel with SiO_2 as the dielectric.

iii] Since the gate is insulated from the channel, the mosfet is sometimes called insulated - gate FET (IGFET)

iv] It is usual practice to connect the substrate to the source (S) internally so that a MOSFET has three terminals that is source (S) gate (G) and drain (D)

v] Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. Therefore D-MOSFET can be operated in both depletion mode and enhancement mode.



Drain characteristics for a depletion type of MOSFET

* Working of D-MOSFET :

i] When $V_{GS} = 0V$, a significant current flows for a given V_{DS}.

ii] When the gate is made negative, the other plate, the channel has a positive charge induced in it opposite the gate this serves to deplete the channel of majority carriers (electrons) so that conductivity decreases, giving rise to characteristics curves like that JFET.

iii) When the gate is made positive, the other plate, the channel has negative charge induced the channel majority charge carriers. So that the conductivity and enchancing current flows

5] The point A acts as voltage divider point for the resistance R_{BB}

6] let the voltage drop across resistance R_{B1} is V_A. According to voltage divider rule.

$$V_A = \left[\frac{R_{B1}}{(R_{B1} + R_{B2})}\right] V_{BB}$$

$$V_A = \eta V_{BB}$$

7] The η is called as intrinsic stand off ratio and it value lies in the range of 0.5 and 0.85.

$$\therefore \eta = \left[\frac{R_{B1}}{(R_{B1} + R_{B2}}\right]$$

2] Explain the parameters of JFET.

→ i] A.C. drain resistance (r_d):

It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate source voltage.

AC drain resistance, $r_d = \frac{\Delta V_{DS}}{\Delta I_D}$ at constant V_{GS}

r_d value varies from 10 kΩ to 1 MΩ

ii) Transconductance (g_{fs}):
The control that the gate voltage has over the drain current is measured by transconductance g_{fs}.
it is ratio of change in drain current (ΔI_D) to the change in gate-source voltage (ΔV_{GS}) at constant drain-source voltage.

$\therefore g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}$, at constant V_{DS}

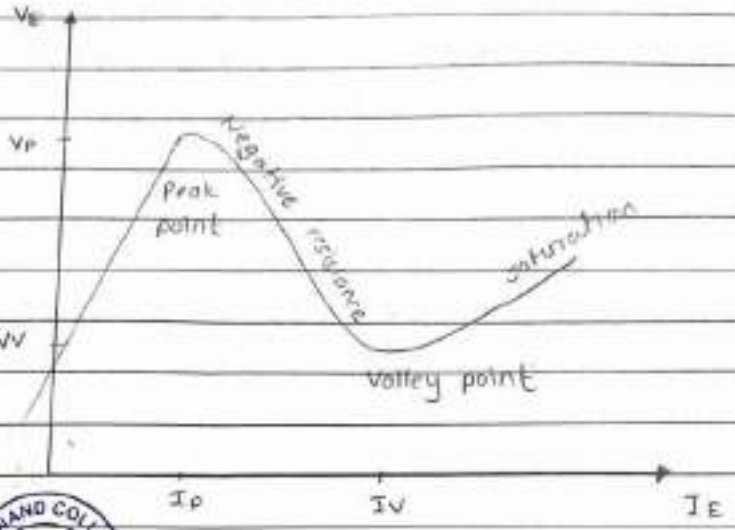
the transconductance is usually expressed either in mA/volt or micromho

iii) Amplification factor (μ):
it is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in gate-source (ΔV_{GS}) at constant drain current.
i.e.

amplification factor, $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$ at constant I_D

'μ' indicates how much more control the gate voltage has over drain current than has the drain voltage.

3] Draw and explain characteristics of UJT



I - V characteristics.

1] The curve between emitter voltage VE and emitter IE of a UJT at a given voltage VBB between the bases, this is known emitter characteristics of UJT.

2] initially in the cut off region, as VE increases from zero, Sight leakage current flows from terminal B2 to the emitter. the current is due to the minority carriers in the reverse based diode.

3] Above a certain value of VE forward current IE begin to flow, increasing until the peak voltage VP and current IP are reached at point P.

4] After the peak point P an attempt to increase VE is followed by sudden increase in emitter current IE with

5] The negative resistance portion of the curve lasts until the valley point Vp is reached with valley point voltage Vv and the valley point current Iv after valley point the device is driven to saturation.

The difference Vp-Vs is a measure of switching effeciency of UJT fall as V_{BB} decreases.

- NAME: Patil Samarth Shrikant
- ROLL NO: 7311
- STD: BSC. FY ● SUB: Electronics

17/30

Q.1 Select correct alternative.

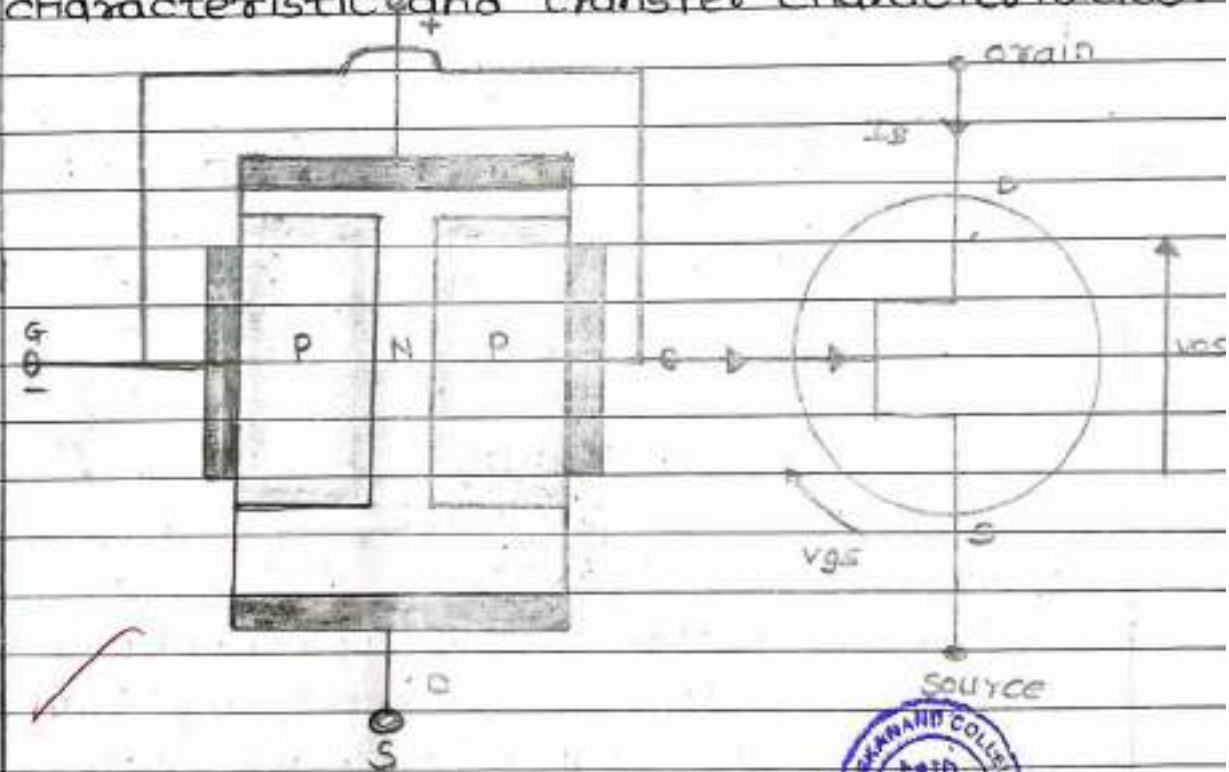
① A JFET is a Voltage driven.

② The input control parameter a JFET is

Q.2 Long answer questions:

i) Explain the N-channel JFET working, drain characteristic and transfer characteristics.

→



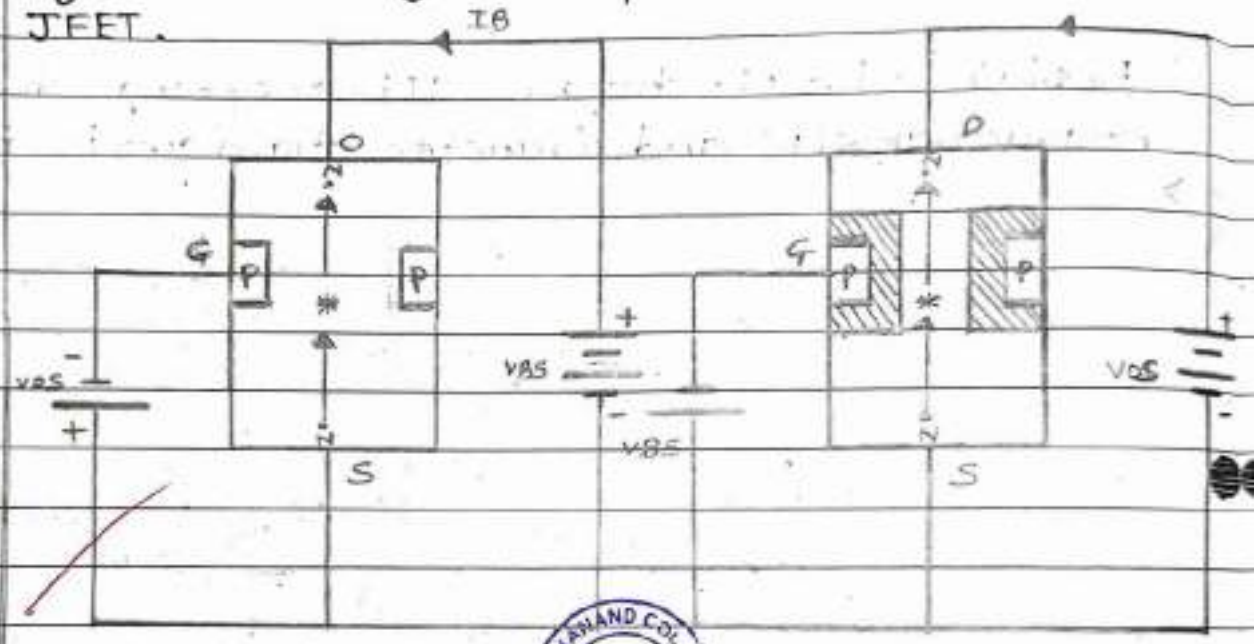
STRUCTURE OF N-JFET

1) A junction field effect transistor is a three terminal semiconductor derives in which current conduction is by on type of carrier i.e. electronics and holes and it is controlled by means of an electric field between the gates elec

trod and the conducting chennel of the device. The JFET has Hight input impendance and low noice level.

2) A JFET consist of a n-type sillicon bar containing two pin junctions of the sides. The bar forms the conducting chennel for the charge carries. If the n-type bar. It is called n-channel JFET.

• fig - Bias voltage for operation of n-channel JFET.



working :

1) when voltage VDS is applied between drain and source and if VGS = 0, then two pin junctions of two sides of stablish depeleation layers. The electrons will flow source to drain through channel between the depletion layers. The size of these layers determines width of the chennel and hence the current conduction through the bar.

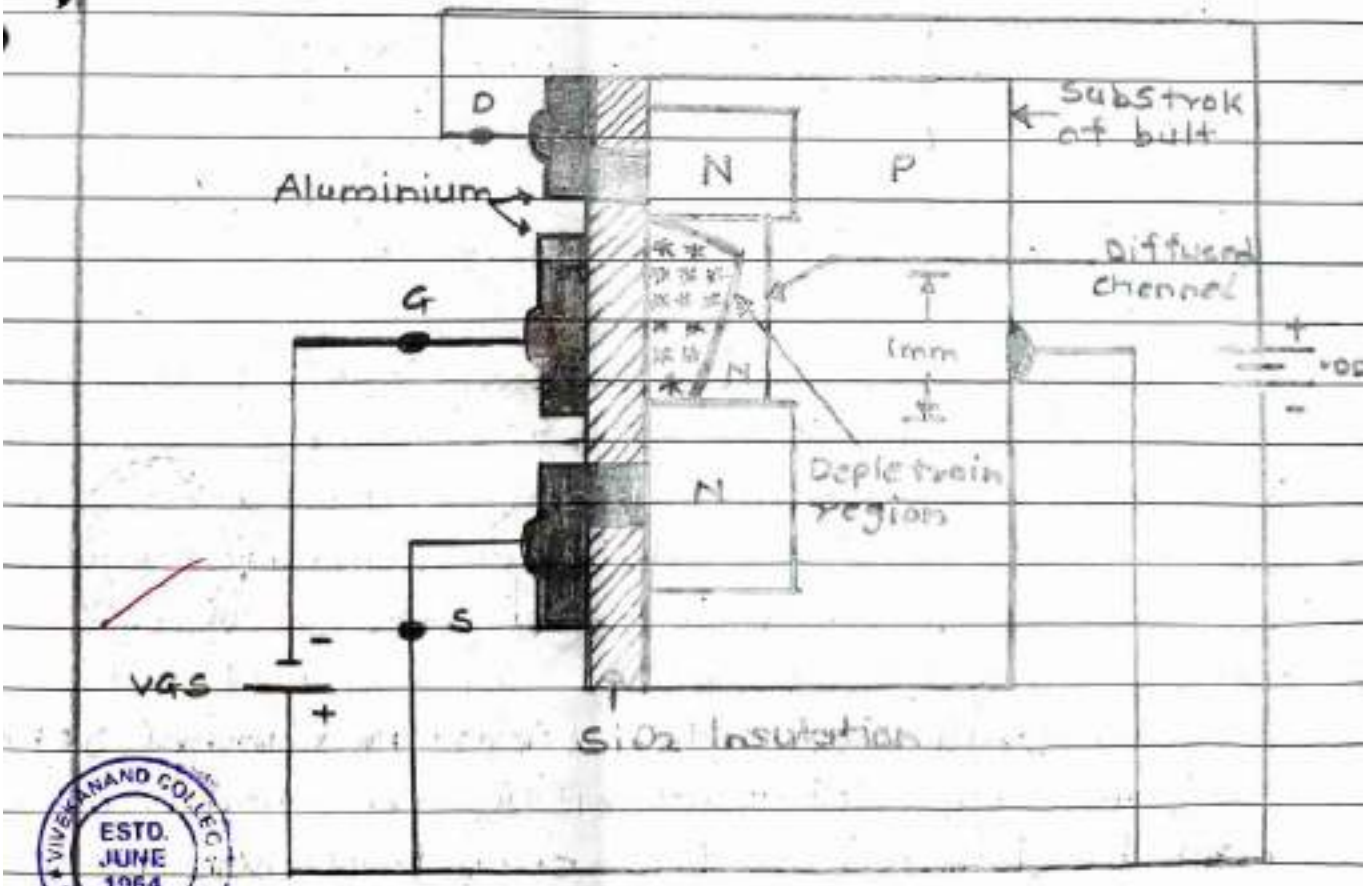
2) when the reverse voltage VGS is applied between the gate and source, the width of

the depletion layer is increased. This reduces the with of chennel and hense current flowing through the chennel reduces. On the other hand it is reverse votage on this gate decreased, the width of depletion layer also decreases resulting in the increase in width of the conducting chennel. Hence the current flowing through circuit increasen.

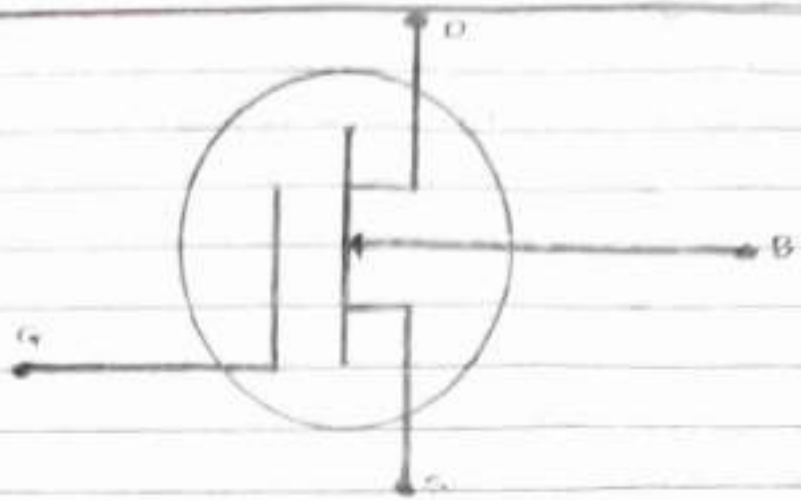
3) If the reverse voltage VGS on the gate is continualy increased, a state reached when the two depletion layers touch each other and the chennel is fulley blocked due to which no current flows through the chennel. The value of this reverse voltage VGS of which the drain current becomes zero is known as VGS (OFF).

ii) Give the construction and working of D-MOSEFT. Also draw its drain characteristics.

→



D-Type MOSEFT Construction.

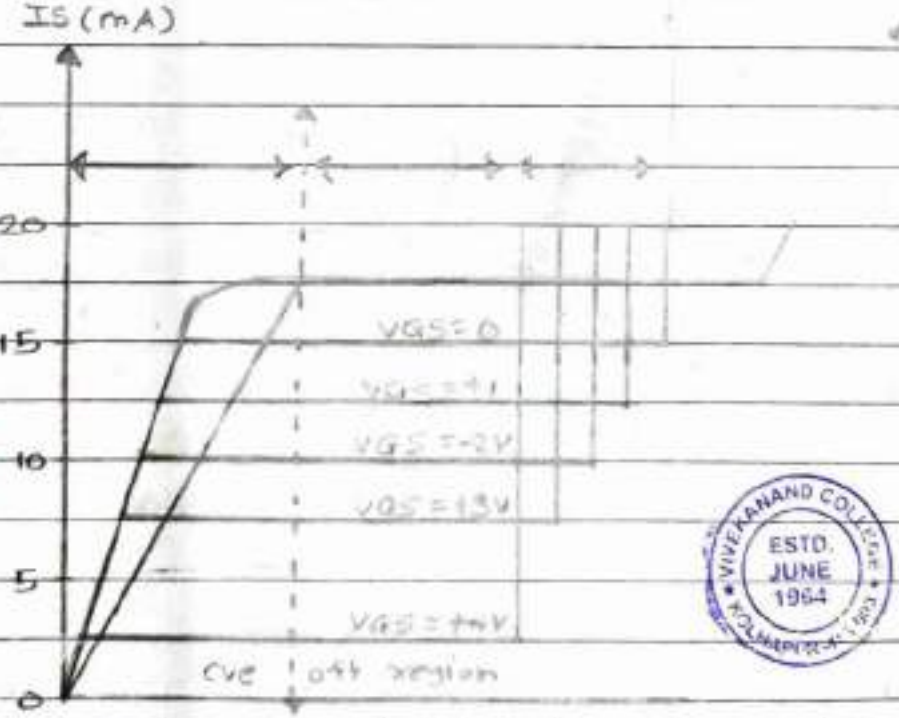


D-Type MOSFET Symbol.

Construction :

i) The n-channel D-MOSFET is a plece n-typ material diffused in a p-type region (called substrate) and an insulated gate on the lef as shown in fig. The free electrons flowing from source to drain must pass through the narrow between the gate and the p-type regi n (i.e substrate)

Drain characteristics :



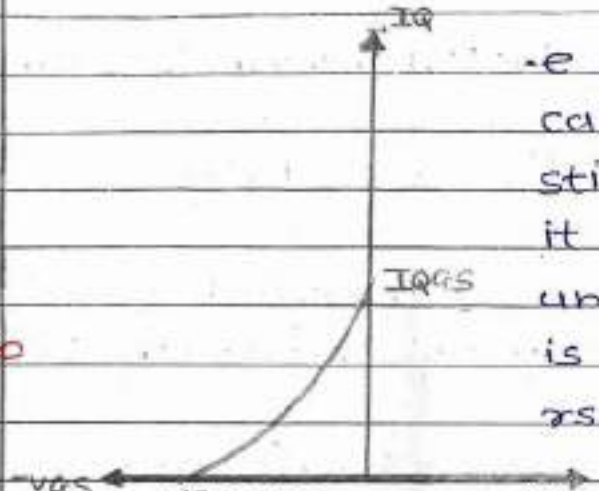
Drain characteristic of n-channel JFET

The output characteristic are shown, which can be defined as the graph between the output current I_D and output voltage V_{DS} keeping

that input voltage VGS are shown fig from the graph the following points can be noted. in order to explain typlce shape of output. characteris tics, we select the curve with VGS = 0 which is subdivided in the following regious.

1) Ohmic region :
2) Curve AB (saturation region) :
3) Breakdown region:

Transfer characturistic:



The graph between the current ID and VGS is called transifer characteristic of FET. from the graph it is clear that ID is maximum where VGS = 0 and ID is zero for maximum reverse value of VGS The JFET must be operated below VGS (OFF).

Q.3 Short answer questions :

1) Explain the equivalent circuit of UJT :

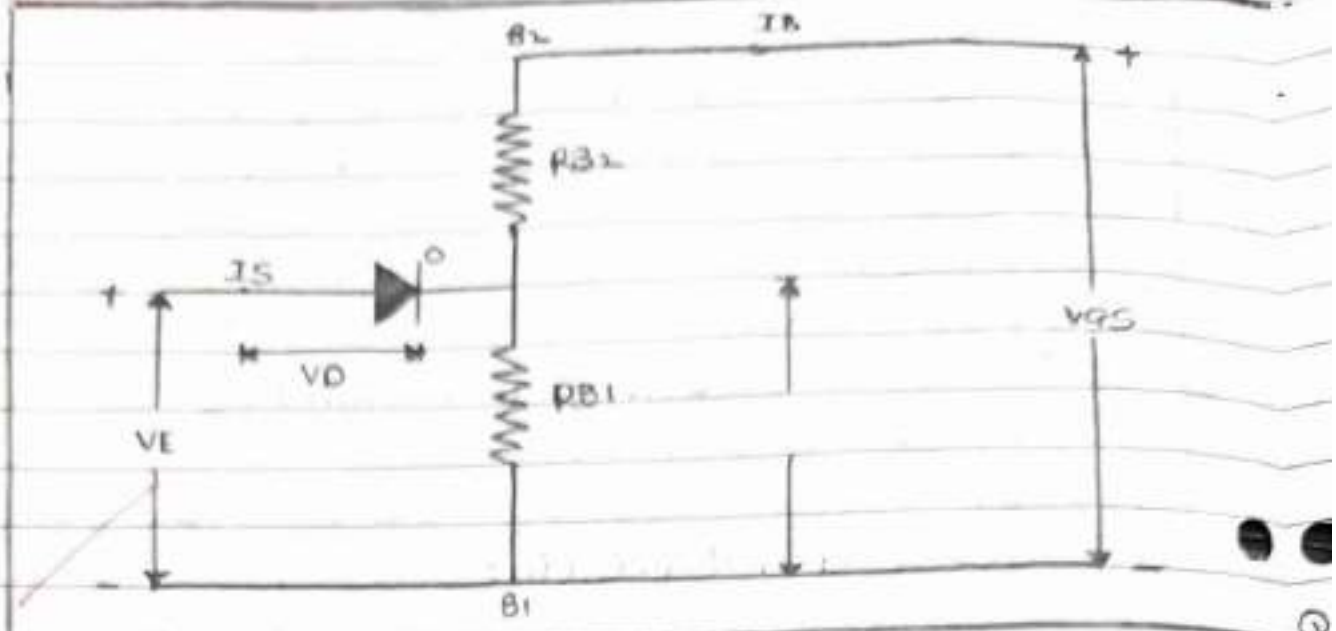
→ The equlvolent circuit of the UJT in shown in fig below the resistance between terminal base 2 with emitter open is called as interbase resistance (RBS).

∴ RBS = RB1 + RB2 where,

RB1 = Resistance between terminal base B1 and emitter.

RB2 = Resistance between terminal base B2 and emitter,

RBB = Interbase resistance.



3 equivalent circuit of the UST intrinsic standoff ratio (η)

1. The value of interbase resistance lines is in the range 5.7 - 10 KΩ
2. R_{B1}, R_{B2} depends upon where the p-type material is located along the n-type bar material.
3. Emitter (E) is closer to base 2 terminal
   ∴ $R_{B2} > R_{B1}$
4. The battery V_{BB} is connected between terminal B_1 and B_2 as shown in fig.

2) Explain the parameters of JFET.

→ (i) A.C drain resistance (r_d):

It is the ratio of change in drain voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate source voltage.

Ac drain resistance, $d = \frac{\Delta V_{DS}}{\Delta I_D}$ at constant V_{GS}

2 Yd value varies from 10 KΩ to 1 MΩ

(ii) Transconductance (g_{FS}):

The control that the gate voltage

has over the drain current is measured by transconductance g_{fs}.

It is the of change in drain current (ΔI_D) to the change in gate-source voltage (ΔV_{GS}) at constant drain-source voltage.

$\therefore g_{FS} = \frac{\Delta I_D}{\Delta V_{GS}}$; at constant V_{DS}

Q.3 Draw and explain characteristics of UJT.

→

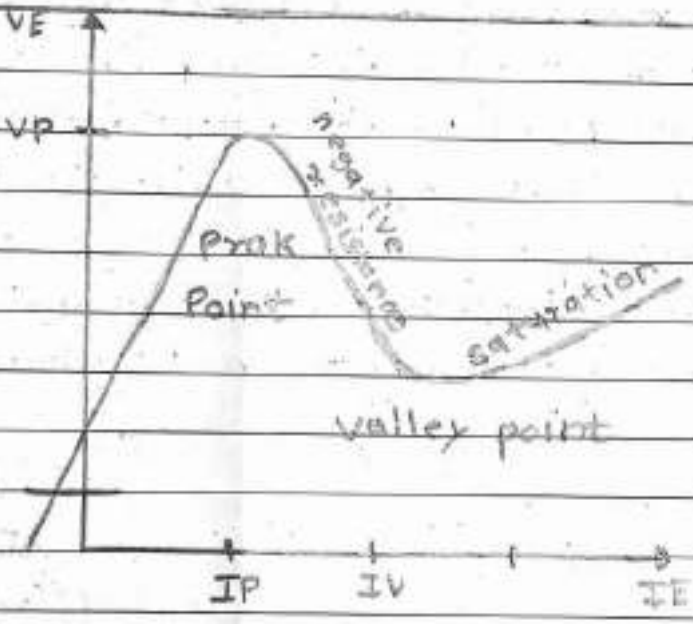


fig - IV characteristic.

- The curve between emitter voltage VE emitter IE of a UJT at a given voltage V_{BB} between the bases. this is known emitter characteristics of UJT.

- Intially cut of region as we increases from zero slight leakage current flows from terminal B_2 to the emitter, the current is due to the emiority carriess in the reverse biased diode.

② Above a certain value of VE forward current IE begin to flow increasing until the peak voltage Vp and current Ip are reached at point p.

③ After the peak point p, an attempt to increase VE is followed by sudden increase in emitter current IE with decrease in VE a negative resistance portion of the curve.

④ The negative resistance portion of the curve lasts until the valley point Vp reached with valley point Vv and the valley point current Iv after valley point the device is driven to saturation.

The difference Vp - Vs is a measure of switching effeciency of UJT fall ∞ VBB decreses.

12/30

Name - Patil Sourabh Bhagawan
Roll no - 7313
Div - A
Subject - Electronics

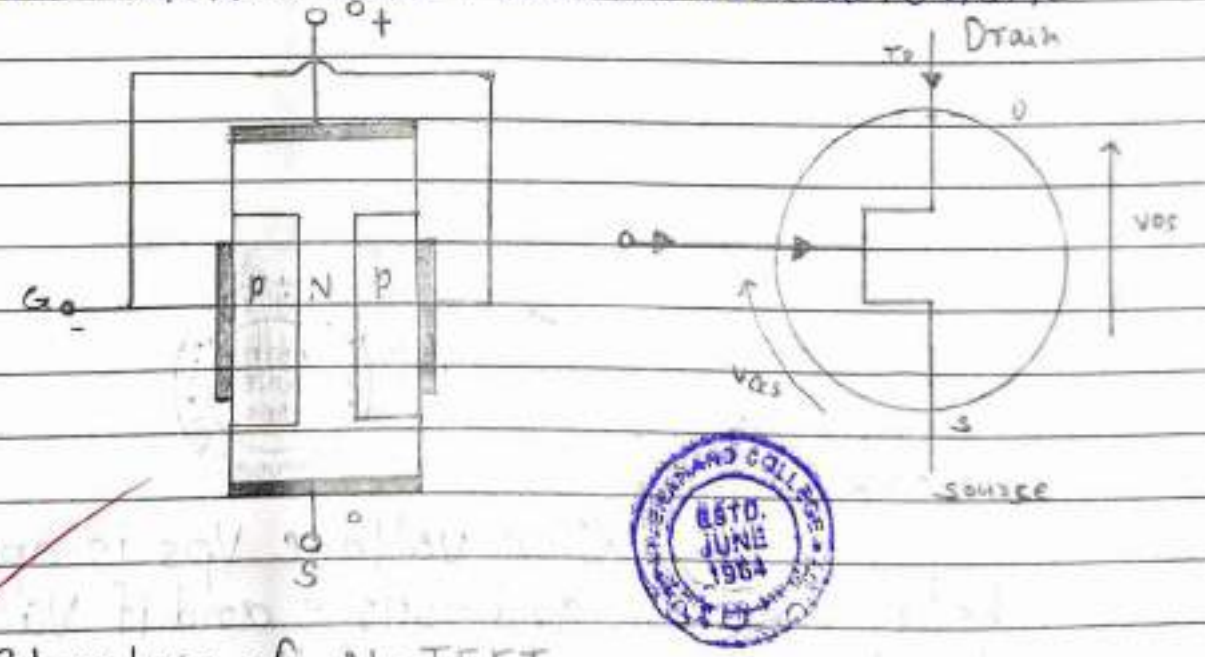
Q 1. Select correct alternative :

1. A JFET is a Voltage driven

2. The input control porometer of a JFET is

Q 2. Long answer question

i) Explain the N - channel JFET working, drain characteristics and transfer charactovistic.

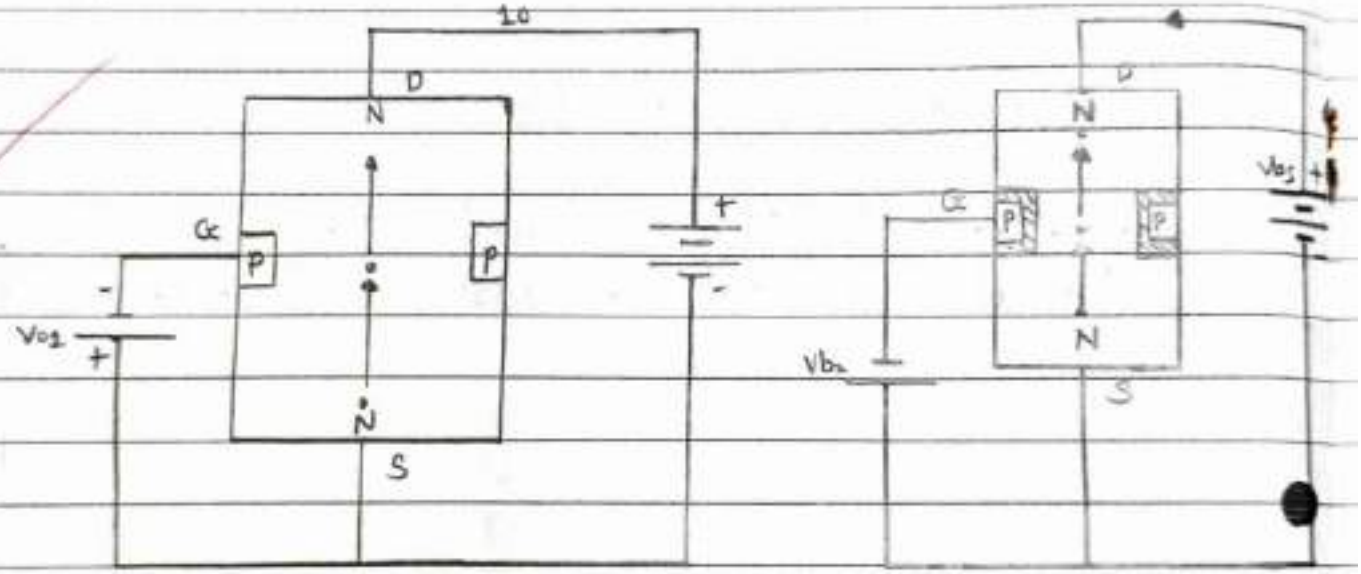


Structure of N-JFET

1) A junction field effect translstor is a theree terminal semiconductor devices in which current conduction is by on type of carrier i.e. electrons and holen and it is conrrolled by means of an

electric field between the gaten electrode and the conducting charmel of the device. The JFET has high input impedance and low noise level.

2) A JFET consists of a n-type silicon bar containing two pin junctions at the sides of the bar forms the conducting channel for the charge carriens. If the bar is n-type. it is called n-channel JFET.



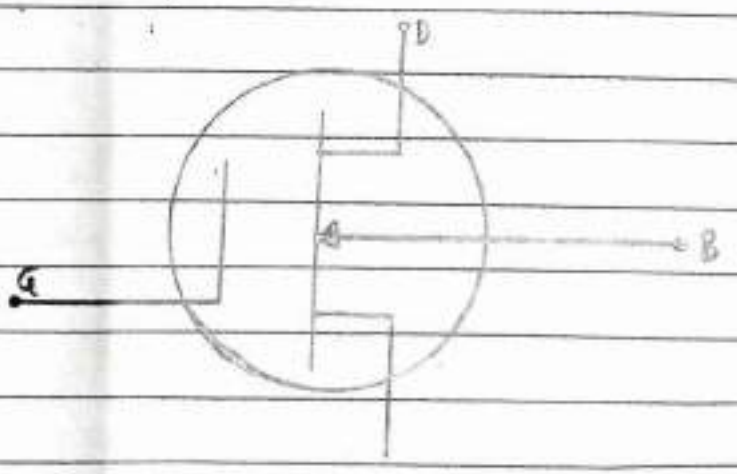
Working :-

1) When voltage Vps is applied between drain and source and if $V_{GS} = 0$, then the two pin junctions of the sides of bar establish depletion layers. The electrons will flow from source to drain through a channel between the current conduction through the bar.

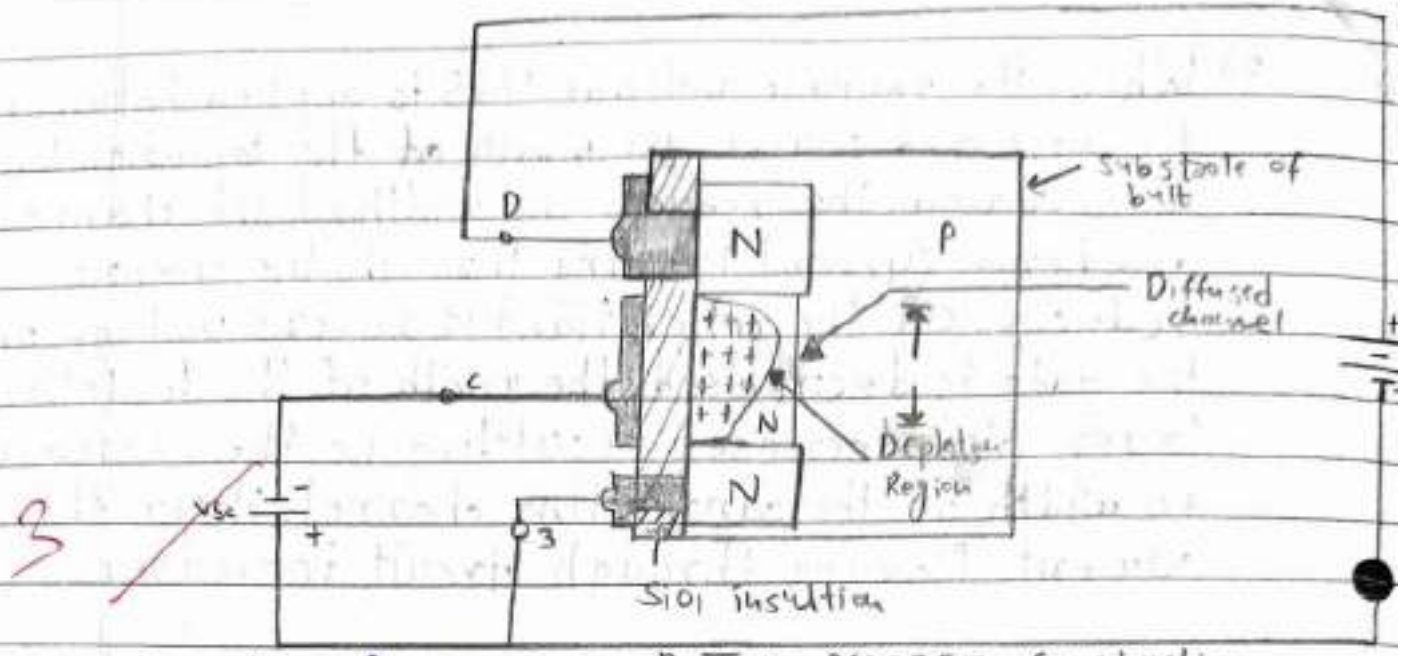
2) When the reverse voltage VGS is applied between the gate and source, the width of the depletion layer is increased. This reduces the width of the channel and hence current flowing through the channel reduces. On the other hand if revene voltage on the gate is decreased, the width of the depletion layer also decreases resulting in the increase in width of the cancluctıng channel. Hence the cuwent flowing through circuit increasen.

3) If the reverse voltage VGS on the gate is continuosdy increased, a stote reoched when the two depletion layers touch eochother and the channel is cut off (pinched off) under such conditions, the channel is fully blocked due to which no current flows through the channel. The value of this reverse voltage VGS of which the drain current becoms zero is known as VGS (off)

ii) Give the construction and working of D-MOSFET. Also drow & drain characteristic and explain it.



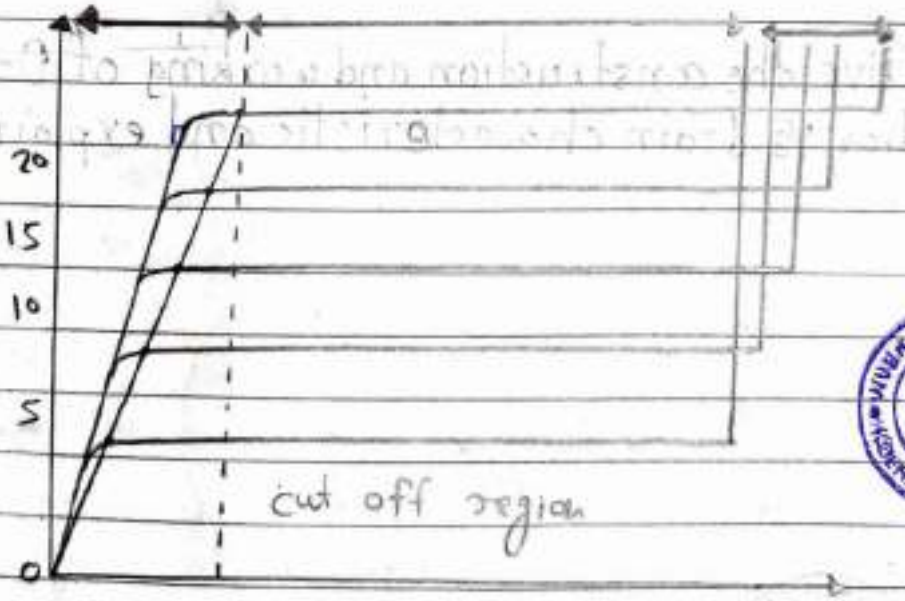
D type MOSFET symbol



D-Type MOSFET Construction

Construction :-

i) The n-channel D-MOSFET is a plece of n-type material diffused in a P type reglon (colled substhlrate) and on insulated gate on the left as shown in fig. The free electhtrons flowing from source to drain must pass through the norrow chan el between the gate and the P-type region. (i.e substrate)



Drain characteristics of n-channel JFET

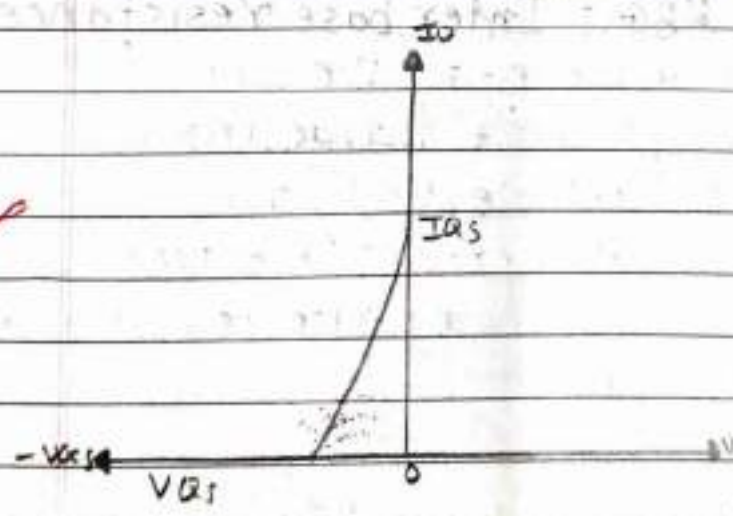
The output characteristics are shown, which can be defined as the graph between the output current Io and output voltage Vds keeping the input voltage VGS constant. The different curves for different values of VGS are shown in fig from the graph the following points can be noted. in order to explain typlee shape of output choro cteri-stice, we select the curve with VGS = 0 which is subdivided in the fellowing regiorus.

1) Ohmic region :-

2) curve AB (saturation region) :-

3) Breakdown region :-

Transfer characteristic :-



The grah between the drain current Io and VGS is called as transf-or charatoristics of FET. from the graph it is clear that Io is maxi-mum when VGS = 0 and Io is zero for masimum reverse value of VGS The JFET must be operated below VGS (off)

Q.3. Short answer questions :

i) Explain the equivalent circuit of UJT.

→

The equivalent circuit of the UJT is shown in fig below the resistance between terminal base 1 and base 2 with emitter open is called as inter-base resistance (RSB)

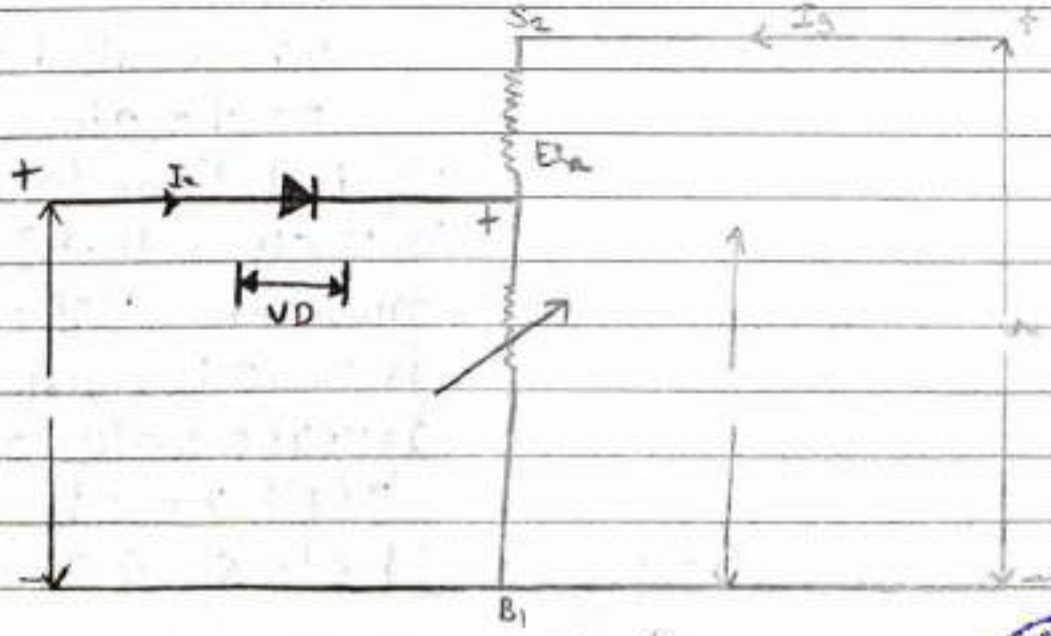
$\therefore RSB = R_{B1} + R_{B2}$

where,

R_{B1} = Resistance between terminal base B_1 and emitter.

R_{B2} = Resistance between terminal base B_2 and emitter.

R_{BB} = Inter base resistance.



1) The value of inter base resistance lies is in the range 4.7 - 10 KΩ

2) R_{B1}, R_{B2} depends upon where the P type material

3) Emitter (E) is closer to base 2 terminal. ∴ $R_{B2} > R_{B1}$

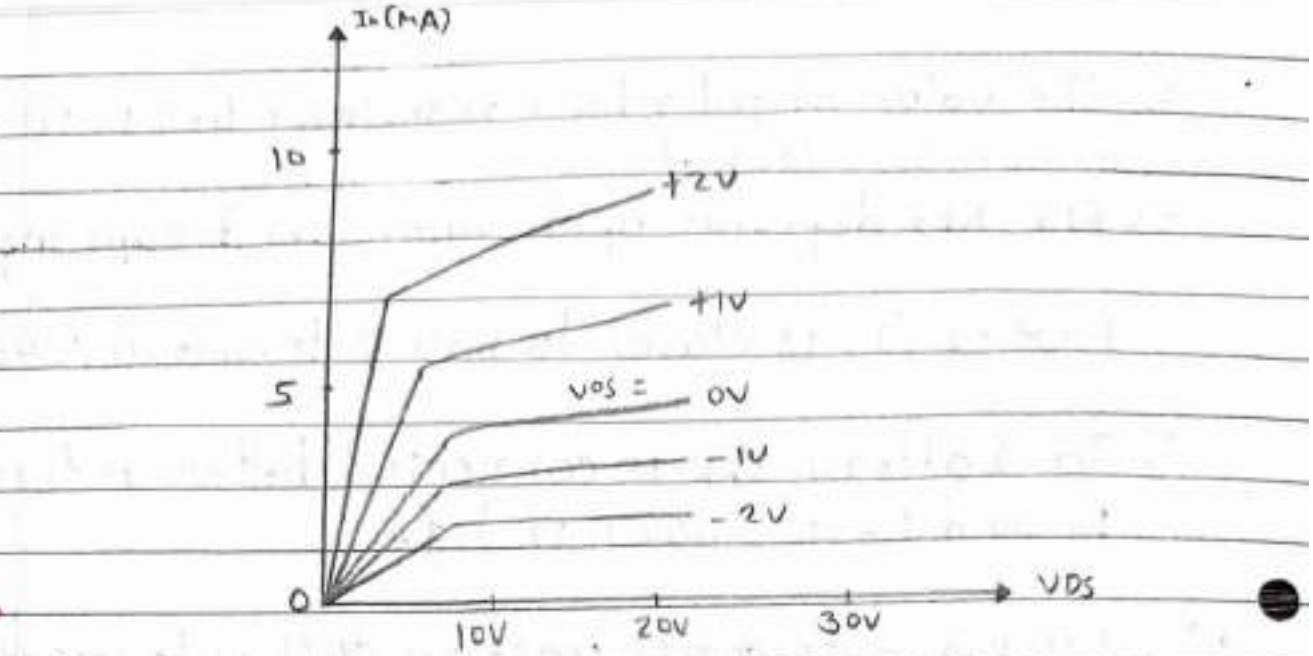
4) The battery V_{BB} is connected between terminal B_1 and B_2 as shown in fig.

ii) During gate construction a thin layer of metal oxide is deposited over a small portion of a channel. A metallic gate is deposited over the oxide layer. As SiO_2 is an insulator, therefore, gate is insulated from the channel. Note that the arrangement forms a capacitor. one plate of this capacitor is the gate and other plate is the channel with SiO_2 as the dielectric.

iii) since the gate is insulated from the channel, the mosfet is sometimes called insulated-gate FET (IGFET).

v) it is usual practice to connect the substrate to the source(S) internally so that a MOSFET has three terminals that is source (S), gate (G) and drain (D)

i) Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. There fore D-MOSFET can be operated in bath depletion made and enhancement mode.



Drain characteristics for a depletion type of MOSFET

WORKING of D-MOSFET :-

i) When $V_{GS} = 0V$, a significant current flows for a given V_{DS}.

ii) When the gate is made negative, the other plate the channel has a positive charge induced in it appasite the gate. This serves to deplete the channel of majority carriers (electrons) so the conductivity decreases, giving rise to characteristic curves like the JFET.

iii) When the gate is made positive, the other plate, the channel has negative charge induced in it appasite the gate. This serves to ~~deplete~~ enhances the channel of majority ~~carriers (electrons)~~ charge so the conductivity ~~decreases, giving rise to characteristic curves like the JFET~~. increcuses and enshancing carrent flows.

6) The point A acts as voltage divider point for the resistance R_{SB}

> let the voltage drop across resistance R_{S1} is V_A Pres According to voltage divider di rule.

$$V_A = \left[\frac{R_{B1}}{(R_{B1}+R_{B2})}\right] V_{BB}$$

$$V_A = \eta V_{BB}$$

7) The η is called as intrinsic standoff ratio and its volus lies in the range of 0.5 and 0.85

$$\therefore \eta = \left[\frac{R_{B1}}{(R_{B1}+R_{B2})}\right]$$

2) Explain the Parameters of JFET.

→

i) A.C. drain resistance (rd):

It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) of constant gate source voltage.

Ac drain reststance, $vd = \frac{\Delta V_{DS}}{\Delta I_D}$ at constant V_{GS}

vd value varies from 10K-Ω to 1MΩ.

ii) Transconductance (g_{fs}):

The control that the gate voltage has over the drain current is measured by transconductance g_{fs}.

It is the ratio of change in drain current (ΔI_D) to the change in gate-source voltage (ΔV_{GS}) at constant drain-source voltage.

$$\therefore g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}, \text{ at constant } V_{DS}$$

18/30 Q

Name :- Sanket J Lambe
Roll no:- 7332
Div :-
Subject :- electronics

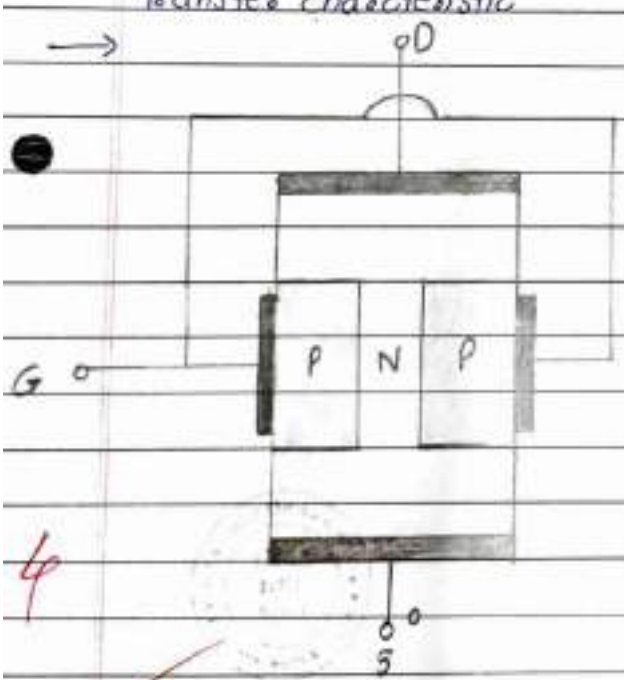
Q.1. Select correct alternative :

1. A JEET is a Voltage driven

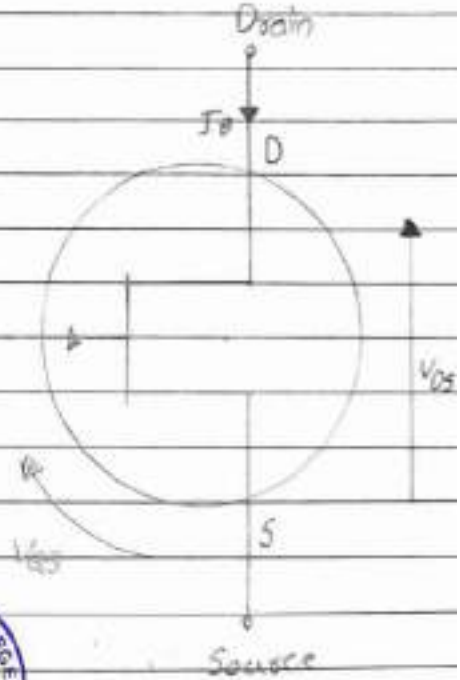
2. The input control parameter of a JEET is

Q.2. Long answer question

i) Explain the N-channel JEET working, drain characteristics and transfer characteristic



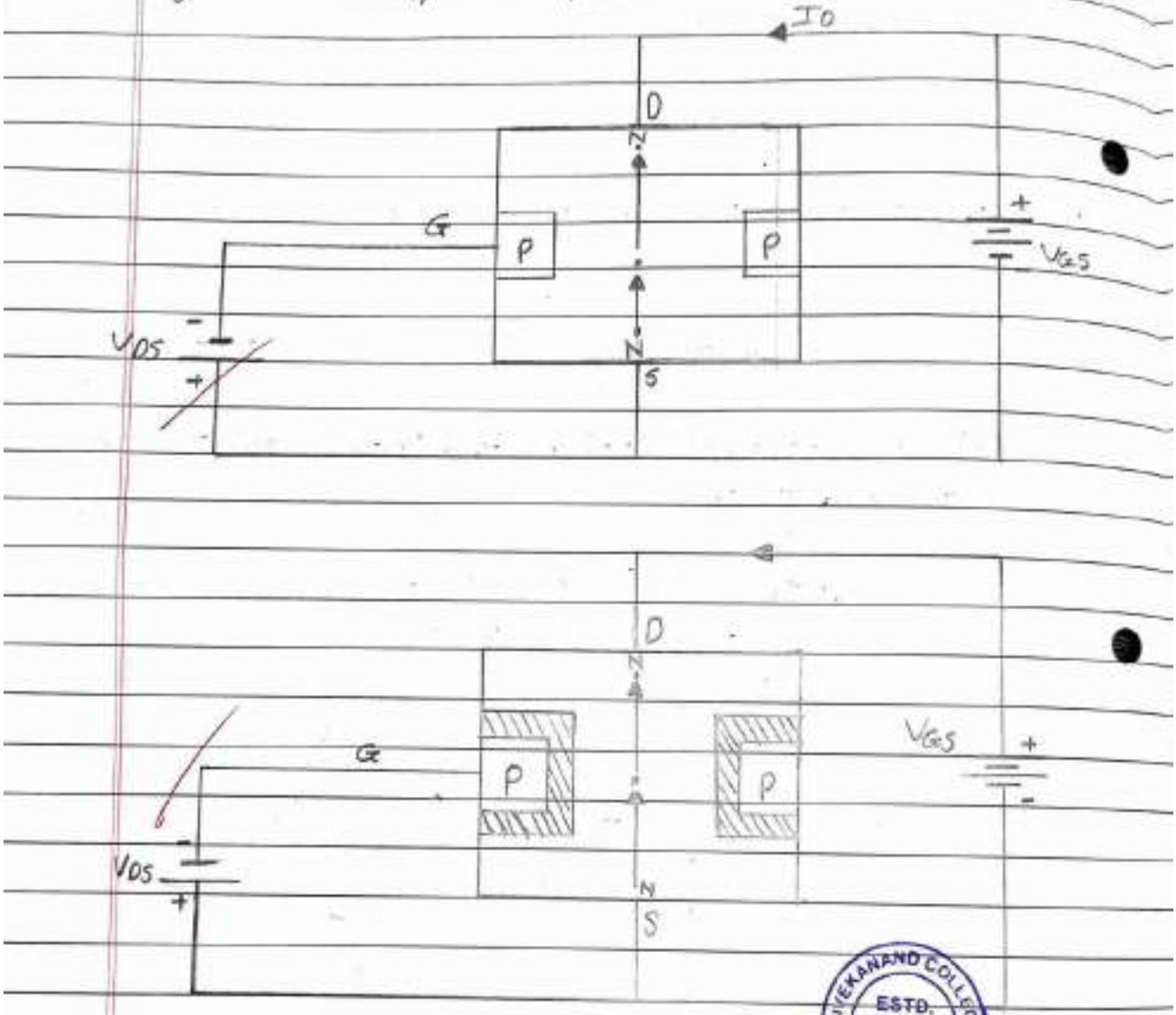
STRUCTURE OF N-JEET



1) A junction field effect transistor is a three terminal semiconductor devices in which current conduction is by on type of carries i.e. electrons and holes and it is controlled by means of an electric field between the gates electrode and the conducting channel of the device. The JFET has high input impedance and low noise level.

2) A JFET consists of a n-type silicon bar containing two pn junctions at the sides of. The bar forms the conducting channel for the charge carriers. If the bar is n-type it is called n-channel JFET

Fig :- voltage for operation of n-channel JFET



working :-

1) When voltage V_{DS} is applied between drain and source and if $V_{GS} = 0$, then the two p/n junctions at the sides of bar establish depletion layers. The electrons will flow from source to drain through a channel between the depletion layers

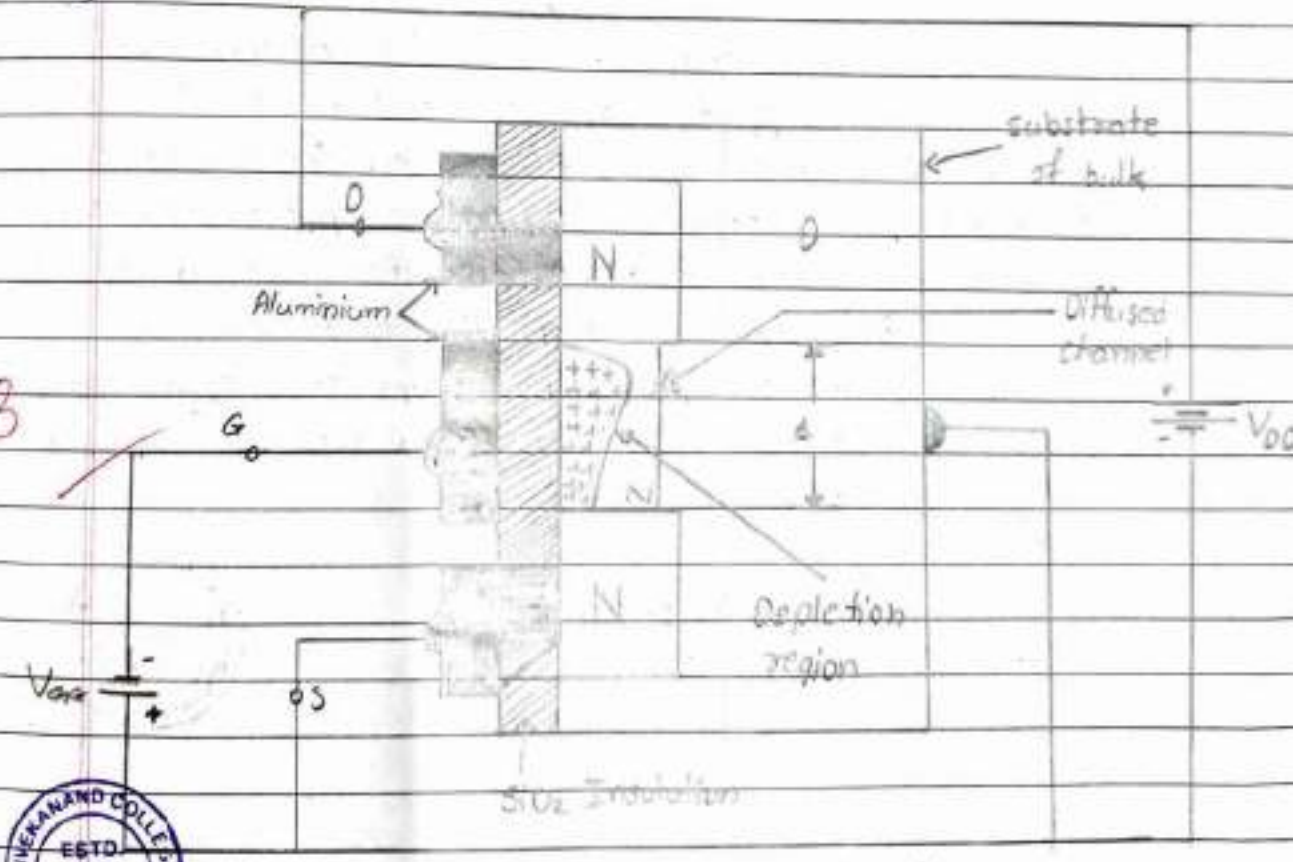
The size of these layers determines the width of the channel and hence the current conduction through the bar.

2) When the reverse voltage V_{GS} is applied between the gate and source, the width of the depletion layer is increased. This reduces the width of the channel and hence current flowing through the channel reduces. On the other hand if reverse voltage on the gate is decreased the width of the depletion layer also decreases resulting in the increase in width of the conducting channel. Hence the current flowing through circuit increase.

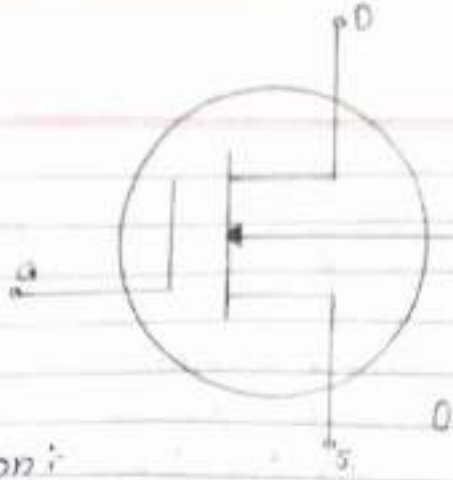
3) If the reverse voltage V_{GS} on the gate is continuously increased, a state reached when the two depletion layers touch eachother and the channel is cutoff (pinched off) under such conditions, the channel is fully blocked due to which no current flows through the channel. The value of this reverse voltage V_{GS} of which the drain current becomes zero is known as $V_{GS}(OFF)$.

ii) Give the construction and working of D-MOSFET. Also draw its drain characteristic and explain it.

→



D-Type MOSFET construction.

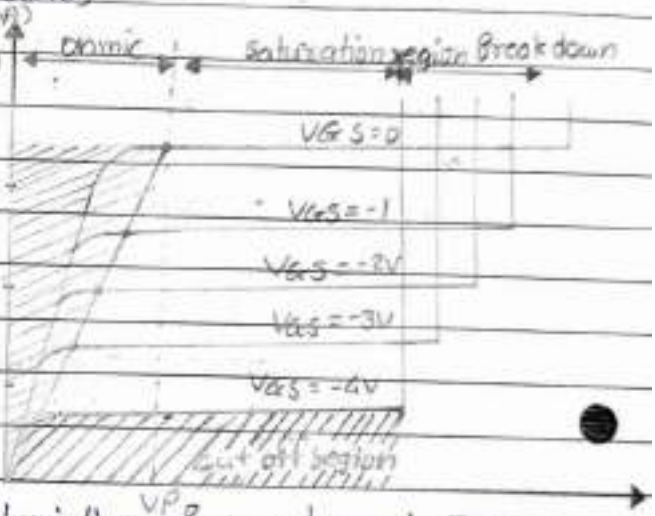


D-Type MOSFET Symbol

Construction:

i) The n-channel D-MOSFET is a piece of n-type material diffused in a p type region (called substrate) and an insulated gate on the left as shown in fig. The free electrons flowing from source to drain must pass through the narrow channel between the gate and the p-type region. (i.e. substrate)

Drain Characteristics :-



Drain characteristics of n-channel JFET

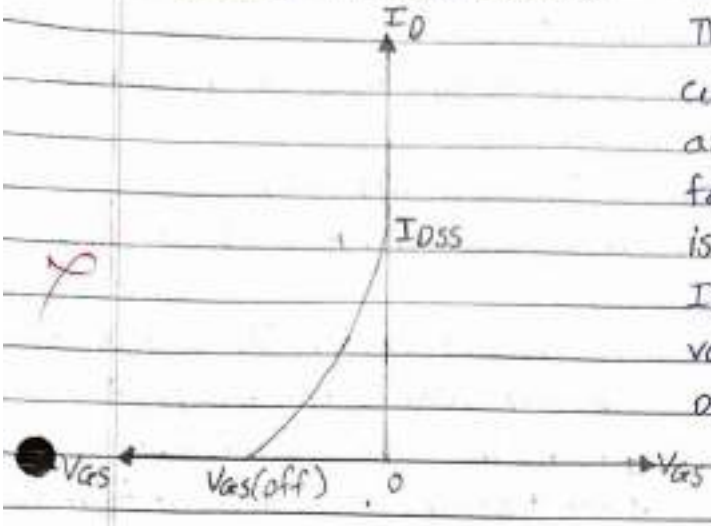
The output characteristics are shown, which can be defined as the graph between the output current I_D and output voltage V_{DS} keeping the input voltage V_{GS} constant. The different curves for different values of V_{GS} are shown in fig from the graph the following points can be noted. In order to explain typle shape of output characteristics, we select the curve with $V_{GS}=0$ which is subdivided in the following regions.

1) Ohmic region:-

2) Curve AB (saturation region):-

3) Breakdown region :-

Transfer characteristic :-



The graph between the drain current I_D and V_{GS} is called as transfer characteristics of FET from the graph it is clear that I_D is maximum when $V_{GS} = 0$ and I_D is zero for maximum reverse value of V_{GS}. The JFET must be operated below $V_{GS(off)}$

Q.3. Short answer questions :-

1) Explain the equivalent circuit of UJT.

→

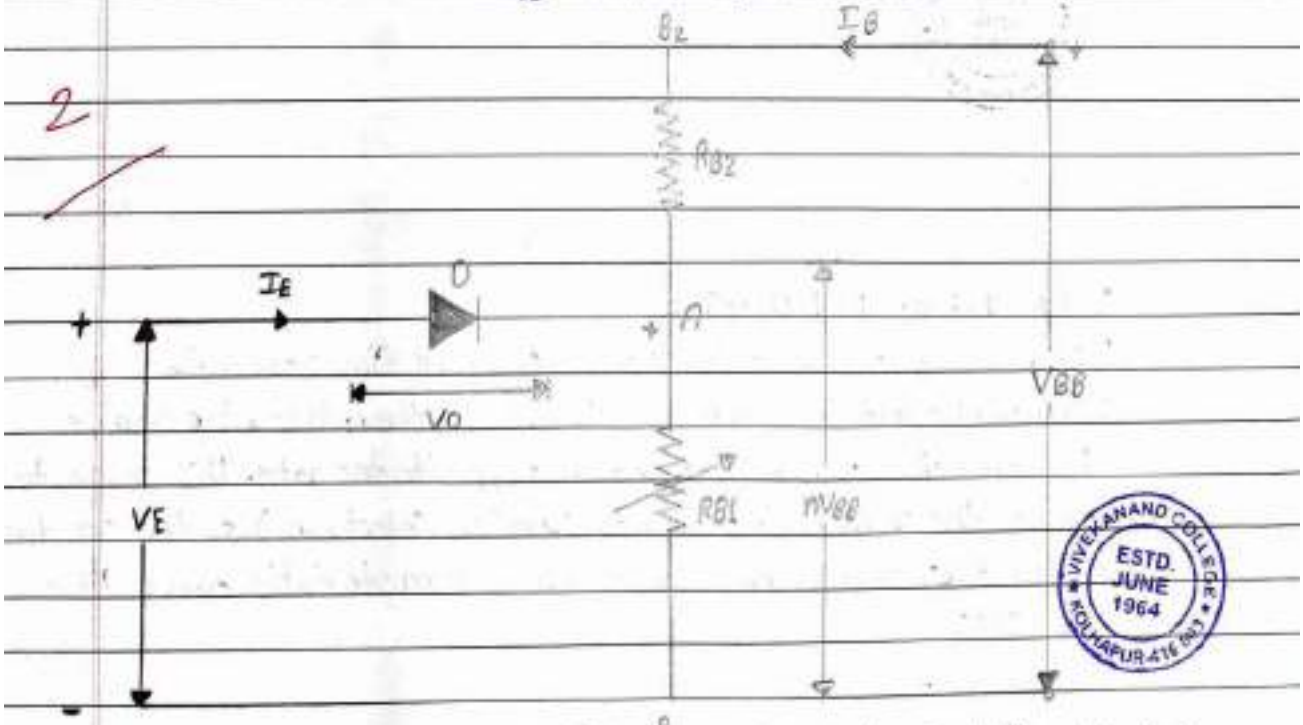
The equivalent circuit of the UJT is shown in fig below the resistance between terminal base 1 and base 2 with emitter open is called as inter-base resistance (R_{BB})

$\therefore R_{BB} = R_{B1} + R_{B2}$

R_{B1} = Resistance between terminal base B_1 and emitter

R_{B2} = Resistance between terminal base B_2 and emitte

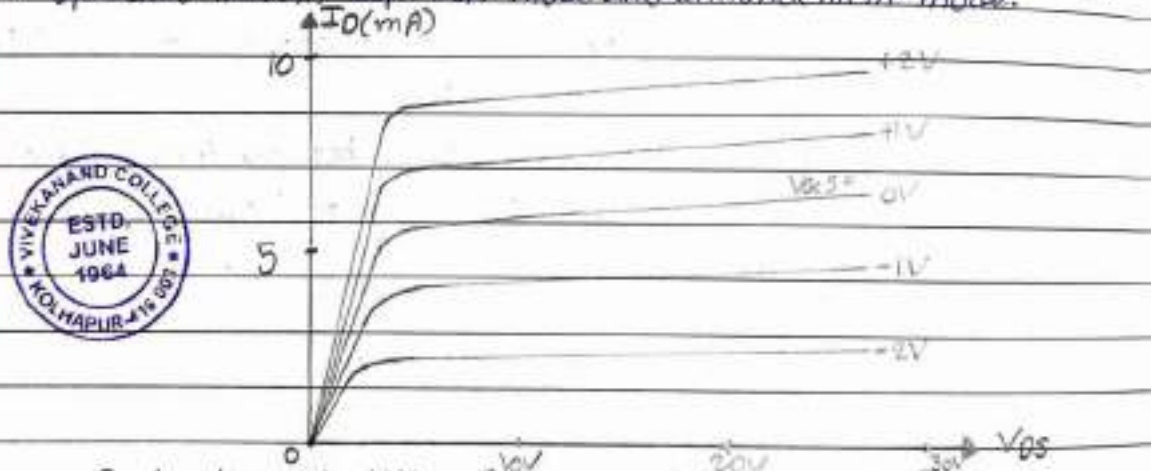
R_{BB} = Interbase resistance



equivalent circuit of the UJT intrinsic standoff ratio (η)

1) The value of interbase resistance lies in the range 4.7-10 KΩ.
2) R_{B1}, R_{B2} depends upon where the P type material is located along the n-type bar material.
3) Emitter (E) is closer to base 2 terminal $\therefore R_{B2} > R_{B1}$
4) The battery V_{BB} is connected between terminal B_1 and B_2 as shown fig.

ii) During gate construction a thin layer of metal oxide is deposited over a small portion of a channel. A metallic gate is deposited over the oxide layer. As SiO_2 is an Insulator, therefore, gate is insulated from the channel. Note that the arrangement forms a capacitor. one plate of ~~its~~ this capacitor is the gate and other plate is the channel with SiO_2 as the dielectric
iii) Since the gate is insulated from the channel, the mosfet is sometimes called insulated-gate FET (IGFET)
iv) It is usual practice to connect the substrate to the source(S) internally so that a MOSFET has three terminal that is source(S), gate(G) and drain(D)
v) Since the gate is insulated from the channel, we can apply either negative or positive voltage to the gate. Therefore D-MOSFET can be operated in both depletion mode and enhancement mode.



Drain characteristics for a depletion type of MOSFET

WORKING of D-MOSFET :-

i) When $V_{GS} = 0V$, a significant current flows for a given V_{DS}.
ii) When the gate is made negtive, the other plate, the channel has a positive charge induced in it opposite the gate. This serve to deplete the channel of majority carriers (electrons) so the conductivity decreases, given rise to characteristic curve like the JFET.

iii) When the gate is made positive, the other plate, the channel has negative charge induced in it opposite the gate. This serves to enhances the channel of majority charge carriers. So the conductivity increases and enchancing current flows.

iv) The point A acts as voltage divider point for the resistance R_{BB}

v) Let the voltage drop across resistance R_{B1} is V_A According to voltage divider rule.

$$V_A = \left[\frac{R_{B1}}{(R_{B1}+R_{B2})}\right] V_{BB}$$

$$\therefore V_A = \eta V_{BB}$$

vi) The η is called as intrinsic standoff ratio and its value lies in the range of 0.5 and 0.85

$$\therefore \eta = \left[\frac{R_{B1}}{(R_{B1}+R_{B2})}\right]$$

2) Explain the Parameters of JFET

→ i) A.C. drain resistance (rd):

It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate source voltage

$$\text{AC drain resistance, } r_d = \frac{\Delta V_{DS}}{\Delta I_D} \text{ at constant } V_{GS}$$

r_d value varies from 10kΩ to 1MΩ

ii) Transconduct (g_{fs}):

The control that the gate voltage has over the drain current is measured by transconductance g_{fs}.

It is the ratio of change in drain current (ΔI_D) to the change in gate-source voltage (ΔV_{GS}) at constant drain-source voltage.

$$\therefore g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}, \text{ at constant } V_{DS}.$$

the transconductance is usually expressed either in mA/volt or micromho.

iii) Amplification factor(μ):

It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in gate-source voltage (ΔV_{GS}) at constant drain current i.e.

amplification factor, $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$ at constant I_D

'μ' indicates how much more control the gate voltage has over drain current than has the drain voltage.

3) Draw and explain characteristics of UJT

→

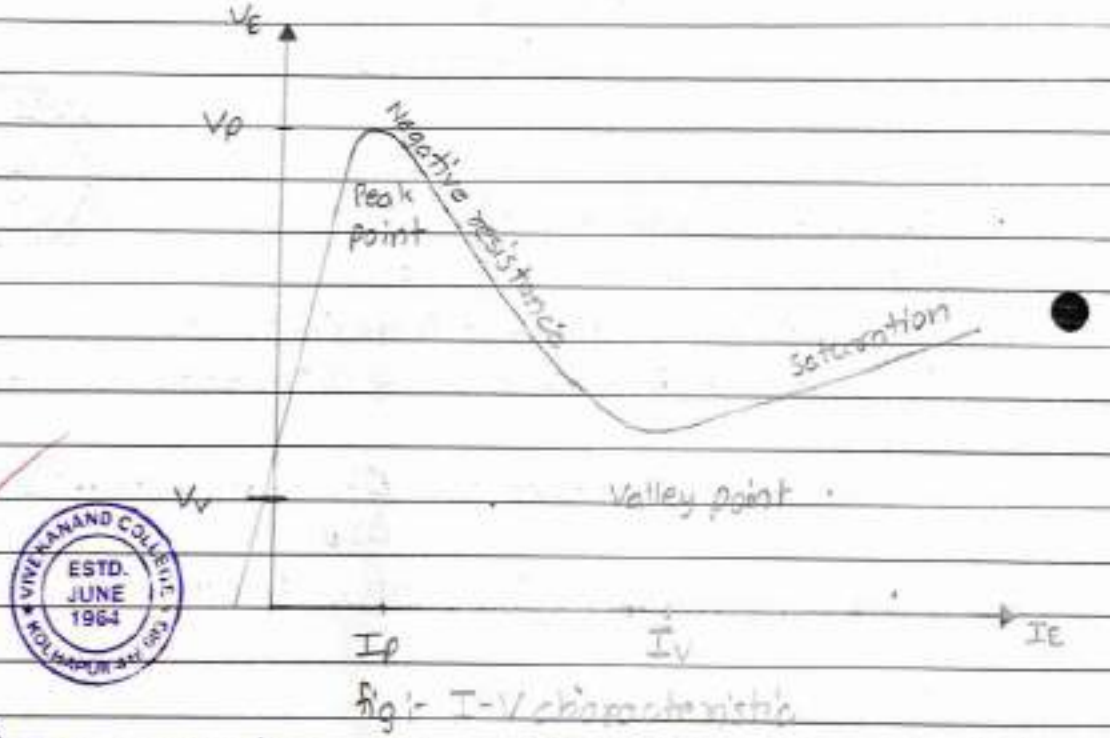


fig:- I-V characteristics

1) The curve between emitter voltage V_E and emitter I_E of a UJT at a given voltage V_{BB} between the bases, this is known emitter characteristics of UJT

2) Initially in the cut off region, as V_E increases from zero, slight leakage current flows from terminal B_2 to the emitter, the current is due to the minority carriers in the reverse biased diode

3) Above a certain value of V_E forward current I_E begin to flow, increasing until the peak voltage V_p and current I_p are reached at point P.

4) After the peak point P an attempt to increase V_E is followed by sudden increase in emitter current IE with derease in V_E is a negative resistance portion of the curve.

5) The negative resistance portion of the curve lasts until the valley point V_p is reached with valley point voltage V_v and the valley point current I_v after valley point the device is driven to saturation. The difference $V_p - V_s$ is a measure of switching effeciency of UJT fall as V_{BB} deacreses.