Vivekanand College, Kolhapur (Empowered Autonomous) Department of Electronics

Date: 04/09/2023

Notice (B.Sc-I Electronics)

All the students of B.Sc-I Electronics are hereby informed that they should write a Home assignment on Unit II (Logic Gates, Boolean algebra) of Digital Electronics-I of total 15 marks and submit to the department on or before 11/09/2023.

Q.1 Short answer questions:

- i) Explain any two basic gates with their logic diagram, truth-table and write boolean equations for them (4 marks).
- ii) Explain derived gates with their logic diagram, truth-table and write boolean equations for them (3 marks).

Q.2 Long answer questions: [8 marks]

i) State and prove De-Morgan's theorems with logic symbol and truth-table.

Subject Teacher

(Dr. P. S. Jadhav)

Head of the Department

Dr. C. B. Patil

HEAD
DEPARTMENT OF ELECTRONICS
VIVEKANAND COLLEGE, KOLHAPUR
(EMPOWERED AUTONOMOUS)



VIVEKANAND COLLEGE, KOLHAPUR (EMPOWERED AUTONOMOUS) B.Sc - I Electronics Roll Call - 2023 - 24

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Ass	gament

Sr.N	Roll			Sub.	
0.	No.	Student Name	Group	Total	
1	7250	ATHANE SHREYA DEE[AK	E.P.M.	1	SOAMORE
2	7251	DESAI SARTHAK SAGAR	E.P.M.	2	Not sub visited
3	7252	KALEKAR HARSH VINAYAK	E.P.M.	3	VPBSD.
4	7253	KAMBLE PRAJWAL KIRAN	E.P.M.	4	Kanto
5	7254	KAMBLE SMITAL VILAS	E.P.M.	5	Not submite
46	7255	KATTI PRATHAMESH MAHESH	E.P.M.	6	De la companya della companya della companya de la companya della
7	7256	KAZI MAHAMANDKAIF MAKSUD	E.P.M.	7	Not submitted
8	,7257	KHOPKAR PRATAMESH BABASO	E.P.M.	8	22444
9	7258	MAHTO SURAJKUMAR SUBHASH	E.P.M.	9	Lunga
10	7259	MANE DINESH DATTATRAY	E.P.M.	10	Med subjuitta
11	7260	NIGADE RUPESH MOHAN	E.P.M.	11	Not submitted
12	7261	PAWAR SHREYAS SUBHASH	E.P.M.	12	Sawar.
13	7262	SHINDE RUSHIKESH VINAYAK	E.P.M.	13	块2.
14	7263	WADKAR PRATHMESH ARUN	E.P.M.	14	Not submitted
15	7222	KAMBLE SAMRAT SURESH	M.E.S.	1	Strobe
16	7223	LAD AALOK BAJARANG	M.E.S.	2	Flore,
17	7224	PATIL VISHWAJEET VIJAY	M.E.S.	3	Sulswitten
18	7225	POWAR ANIKET PANDURANG	M.E.Ş.	4	Not supported
19	7264	ATTAR NASHRA ABDULLAH	Comp.E.M	1	NAA:
20	7265	BIRJE NAMRATA NARAYAN	Comp.E.M	2	N. N. BOT
21	7266	CHARANKAR SHARVARI SANJAY	Comp.E.M	3	Maxanta
22	7267	CHOUGULE SWEJAL AMAR	Comp.E.M	4	Ehogua.
23	7268	GAIKWAD URVEE UMESH	Comp.E.M	5	Halkwad
24	7269	GURAV SAHIL SAMIR	Comp.E.M	6	21/11
25	7270	KAMBLE SAKSHI SAGAR	Comp.E.M	7	Monde
26	7271	KAMBLE SHRUTIKA BAPU	Comp.E.M	8	Not sul mitted
27	7272	LAHIGADE PARTH SAGAR	Comp.E.M	9	Blobigade
28	7273	MNGOLI HANNAH DARWIN	Comp.E.M	10	₩.
29	7274	MORBALE VAISHNAVI PARSHRAM	Comp.E.M	11	Wishney
30	7275	PATIL BHAKTI SAMBHAJI	Comp.E.M	12	Production
31	7276	PATIL UTKARSHA NITIN	Comp.E.M	13	ORIL
32	7277	PATIL VIRAJ UTTAM	Comp.E.M	14	THAT
33	7278	PEDANEKAR SHIVAJI SATAPPA	Comp.E.M	15	Sportugues
34	7279	POWAR SANIKA ASHOK	Comp.E.M	16	Simb-
35	7280	SALOKHE HARSHADA SUREDNRA	Comp.E.M	17	Not submitted
36	7281	SAMARTH ALLI ASHRAF	Comp.E.M	18	AShrap
_	7282	SUTHAR MAINA OMPRAKASH	Comp E M	19	MS NUCL
		CHO COLLEGE	40	19	Marie

38	7283	TELEKE NITASI TELEKE	Comp.E.M	20	Neine
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40	7340	AWATE AKASH SURESH	Comp.E.S.	1	Not submitted
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48	7348	MUJAWAR SALIL SIKANDAR	Comp.E.S.	9	PHIMA
49	7349	PATIL MADHURA ANANDA	Comp.E.S.	10	500
50	7350	PATIL SANIKA DAGADU	Comp.E.S.	11	Sahirece
51	7351	PATIL TEJAS POPAT	Comp.E.S.	12	Patil
52	7352	SANKPAL ARATI BABAN	Comp.E.S.	13	& Cark pa
53	7353	SUTAR MANISHA BAJARANG	Comp.E.S.	14	mge_
54	7354	VAGRE ROHAN SANJAY	Comp.E.S.	15	Osragre
55	7355	VEER SNEHAL DILIP	Comp.E.S.	16	Orano

Subject Teacher (Dr. P. S. Jadhav)



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(Dr. C. & Patil)

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DEPARTMENT OF ELECTRONICS

VIVEKANAND COLLEGE, KOLHAPUR

(EMPOWERED AUTONOMOUS)

Shri Swami Vivekanand Shikshan Sanstha's

VIVEKANAND COLLEGE, KOLHAPUR (Empowered Autonomous) B Sc. Electronics-I 2023-24

Home Assignment Marks Entry out of 15

Sem I

DIGITAL ELECTRONICS-I Unit. Logit Gates and Boolean Algebra

Sr. No.	Roll No.	Marks	Sr. No.	Roll No.	Marks
1	7250	15	29	7274	15
2	7251	0	30	7275	14
3	7252	12	31	7276	15
4	7253	14	32	7277	12
5	7254	0	33	7278	11
6	7255	14	34	7279	14
7	7256	0	35	7280	(
8	7257	12	36	7281	13
9	7258	14	37	7282	1:
10	7259	0	38	7283	1
11	7260	0	39	7284	1
12	7261	14	40	7340	
13	7262	15	41	7341	1
14	7263	0	42	7342	1
15	7222	15	43	7343	1
16	7223	14	44	7344	1
17	7224	15	45	7345	1
18	7225	0	46	7346	1
19	7264	15	47	7347	
20	7265	15	48	7348	-
21	7266	15	49	7349	
22	7267	14	50	7350	
23	7268	15	51	7351	
24	7269	9	52	7352	
25	7270	15	53	7353	
26	7271	0	54	7354	
27	7272	12	55	7355	
28	7273	11		1300	

Dr. P.S. Jadhav Subject Teacher



Dr. C. B. Patil

DEPARTMENT OF ELECTRONICS
VIVEKANAND COLLEGE, KOLHAPUR
(EMPOWERED AUTONOMOUS)

Assignment No-1

PAGE NO.:

Sub: Electronics

Name-Namrata Narayan Birde Class- Bec-cs-fy Div !- A' Rou No :- 7265

107

Explain basic gotes with their logic diagram, touth table and write the boolean equation.

Basic (fundamental) gates -

1] or gate

2] AND gate

3] NOT gote

1] OR GATE -

As its name implies, an or logic gate performs on "or" logic operation, which is an addition. It has at least two inputs So, if A and B are its inputs, at the output we will find (A+B) so or logic gate can be Summarized by the formula Y = A+B, "If either A or B is true, then Q is true",

logic <u>Diogram</u>-

Ao

Ba

Q =

Two p input of gate symbol.



(Sule kha)

	il lal-10 -	197 4/		
1	Truth table -		r July	
	Inputs	I Leave &	outputes	
	A	B	Q = A+B	
	13.4.11	1.34		
	0	0	0	
	O		1	
	- 1	0 1,	!	
	1	1 1	1	
	Truth to	able of	or gate.	
	Boolean Equation	<u> </u>		
	\[\text{\chi}_{\chi}\]	2.0		
	YA	A+B		
2]	AND GATE :-			
4		its name	implies, ar	2 220 22
	logic gate pe	rforms o	IN "AND" log	ic occupies
	which in an	mw tiplicat	ion It has	at 10001 110
	Inputs, so it	A and	a and ite in	20110 -1 11-
	Loutbut me	Dill tind	(AXA) Ca A	No 11-
	Core de Julia	HULLIAN L	the torm	110 Y - N = N
	"If both A one	B are	true, then q	is true"
			·	
	Logia Diagram	~		
		1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	U1 1	
	0		12	
	0	7	-9	
	Two ioni	D 10		
- 1	Comment of the	HND got	e Symbol.	
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	图 福江湖			FSTD P
1	V 4 4 387			WINE 18



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1	ruth	toble	•	_

Inputs			outputes
. A	В		outputes Q=A+BAB
0	0	1	O
0	1		1
1	0		1
1	1		1

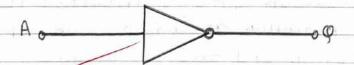
Boolean equation :
Y = A B

3) NOT GATES

As the name implies, inverter will invert the number entered If you enter'o", you will get a"!" on its output, and if you enter o"!" you will get a "o" on its output The inverter Symbol is Shown in fig 2.3.

Inverter gate is also known as Not and it output is Y = A.

Logic Diagram -



Not gate symbol





Truth table -

Input	output
A	$Q = \overline{A}$
0	1
1	0
	1

Truth toble of Not gate

Boolean Equation -

 $Y = \overline{A}$

92 Explain derived gates with their logic diagram
Truth table and write the boolean equation

Derived Gates -

17 NOR gate

2] NAND gate

3] Ex-or gate

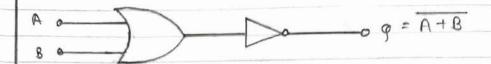
NOR GATE -

Nor gate means Not-or gate. In a Nor gate an or gate is inverted through a Not gate. Actually on inverted or operation is Nor operation and the logic gat performing this operation is colled Nor gate. A Not gate tollowed by an orgate makes a Nor gate the basic logic Construction of the Nor gate is shown below.



PAGE NO).:		7
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100	4
	100
0010	diagnam.
LOGIC	diagram.



a] - Logic circuit of NOR gote.



b] Symbol

Truth table -

Top	its.	output
A '	B	g = A+B
0	0	1
0	1 (0
1	0	0
1	1	O

Truth toble of NOR gate

Booleon Equation -

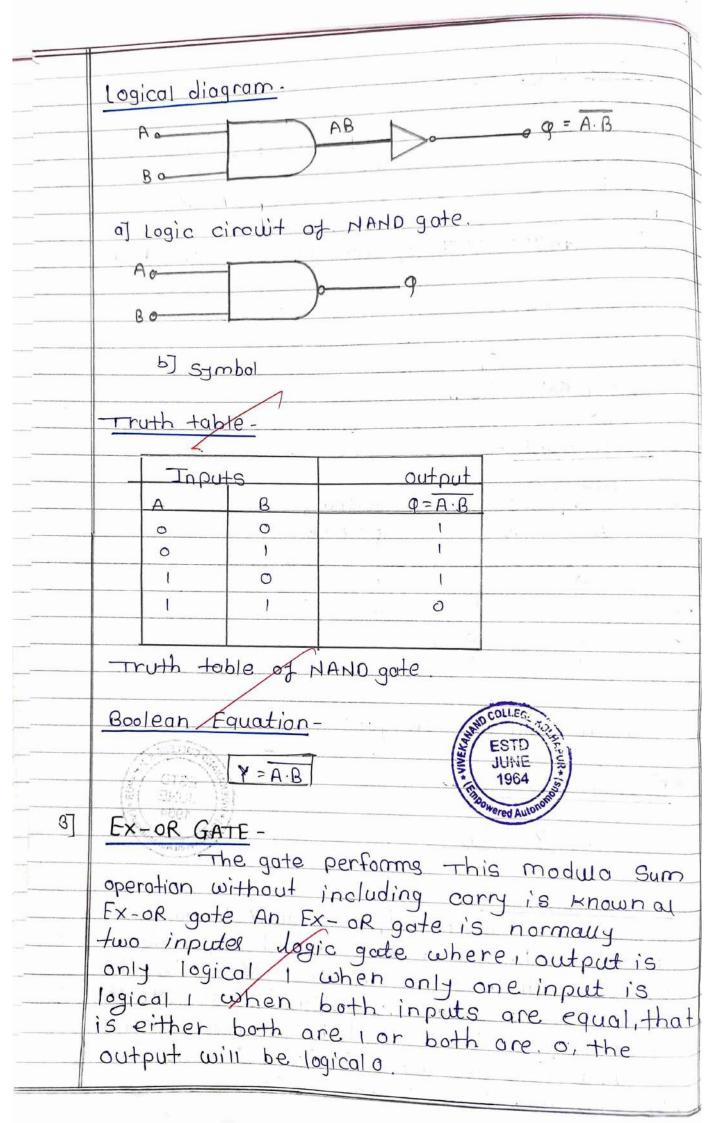
 $Y = \overline{A + B}$

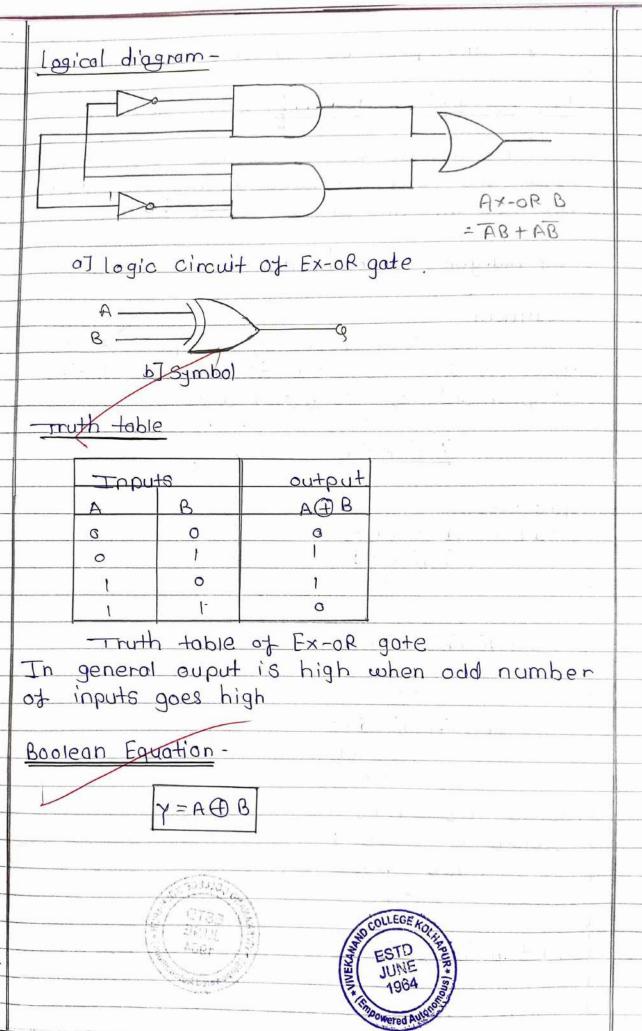


2] NAND GATE -

when output of an AND gate is inverted through a Not gate the aperation is called NAND operation. The logic gate which performs this ANAND operation is called NAND gate A NOT gate Jollowed by an AND gate maker a NAND gate the basic logical Construction of the NAND gate is Shown below.

(Sulekha)





(Suleklic)

93 State and prove De-Margan's Theorem

DE - MORGAN'S THEOREM-

which are extermely used in Boolean algebra The two theorems are discussed below.

· De-margon's first theorem-

Statment

The Complement of the product of two Variobles is equal to the sum of the Complement of each variable.

A.B. A+B

proof
Juhan A = 0, B = 0 $A \cdot B = 0 \cdot 0$ = 0and A + B = 0 + 0 = 1 + 1 = 1

Hence $\overline{A \cdot B} = \overline{A + B}$ 2] when A = 0, B = 1 $\overline{A \cdot B} = \overline{0 \cdot 1}$ $= \overline{0}$



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S) when
$$A = 1$$
, $B = 0$

$$A \cdot B = 1 \cdot 0$$

$$= \overline{D} = 1$$
and $\overline{A} + \overline{B} = \overline{1} + \overline{0}$

$$= 0 + 1$$

Hence
$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

4] when $A = 1$, $B = 1$
 $\overline{A \cdot B} = \overline{1 \cdot 1}$
 $= \overline{1}$

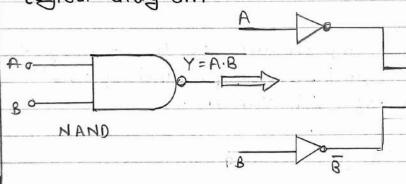
and
$$\overline{A} + \overline{B} = \overline{1} + \overline{1}$$

= $\overline{0} + 0$

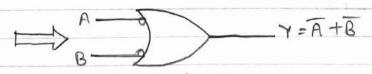
= 0

Hence A.B = A + B

Legical diagram-



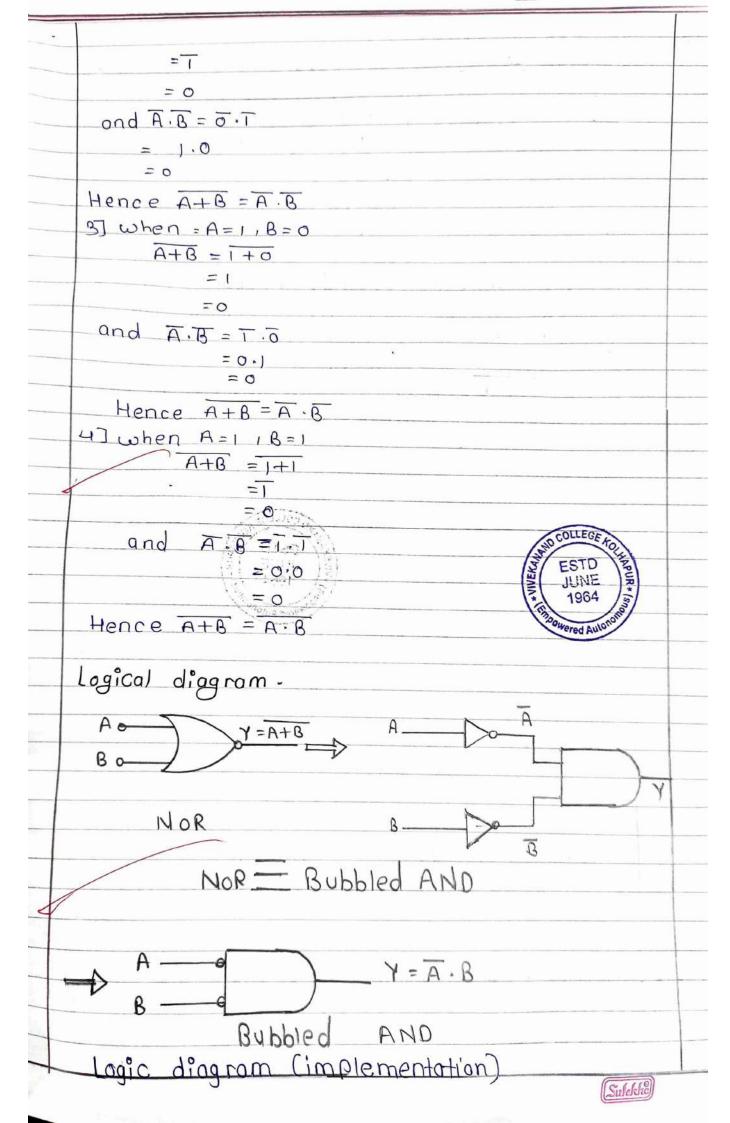
NAND _ Bubbled or



Bubbled or Logical Diogram (Implementation.)



Truth table output Input AB 0 0 Truth toble of first theorem Boolean Equation -A.B = A +B ·De-morgan's Second Theorem -Statmens The Complement of the Sum of two variables is equal to the product of the Complement of each Variable A.B = A.B proof -Juhen A=0, B=0 A+B = 0+0 and A.B = 0.0 ESTD JUNE Hence A+B = A ·B 1964 2] when A=0, B=1 A+B =0+1



Truth toble -

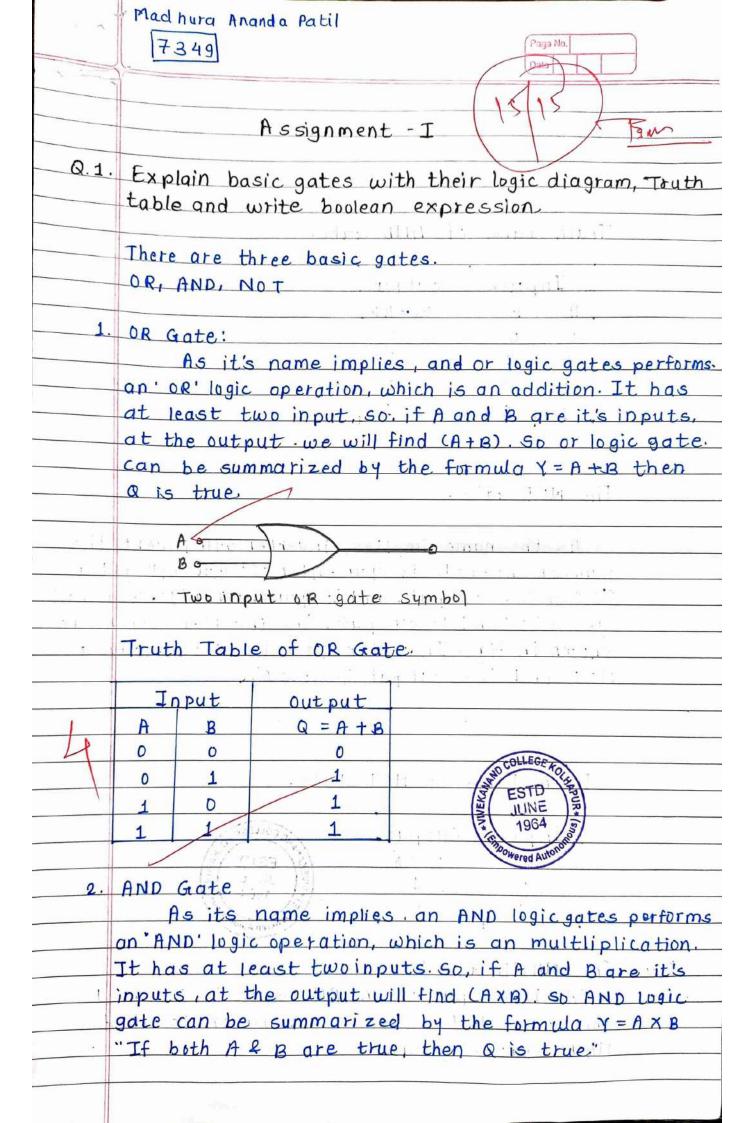
0	B	A+B	A.B
0	0	1	1
0	1	0	0
1	0	0	0
1		0	0

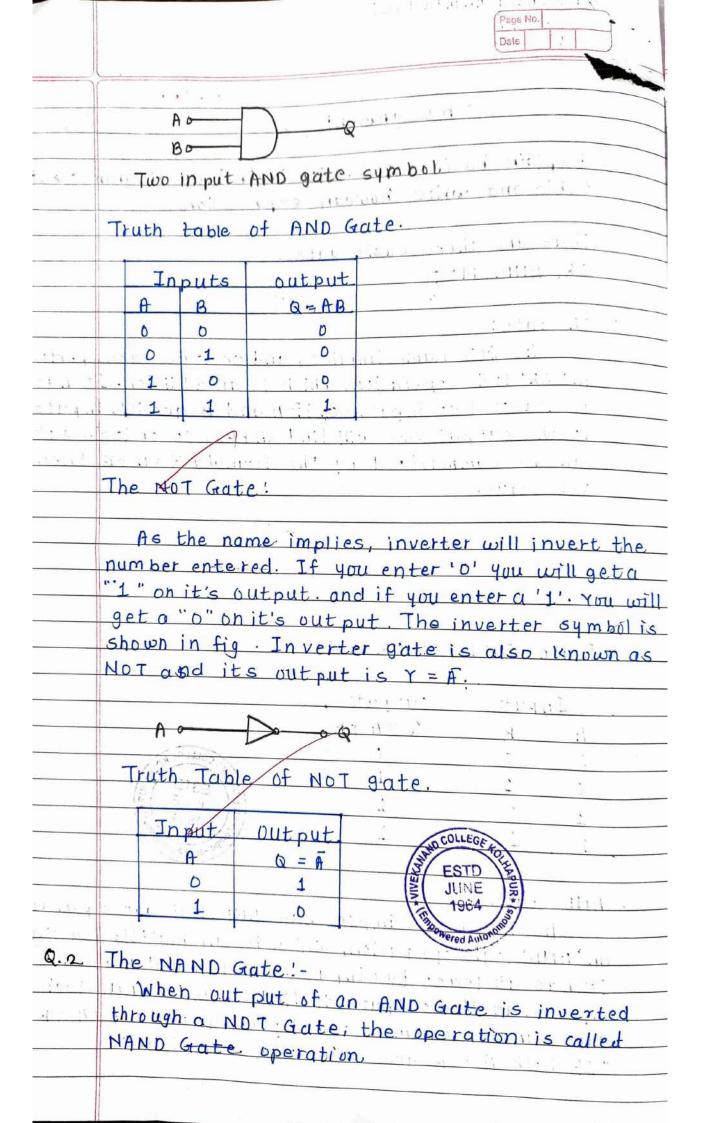
Truth toble of second theorem

Booleon Equation -

A+B = A.B

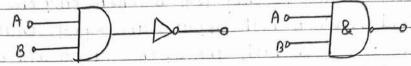








The logic gate which performs this NAND operation is called NAND gate. A NOT gate followed by an AND gate makes a NAND gate. The basic logical construction of the NAND gate is shown below.



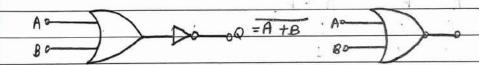
Logic circuit of NAND

symbol

Gate.

The NOR Gate!

NoR gates means NOT-OR gate in a NoR gate, an OR gate is inverted through a NOT gate Actually an inverted or operation is NoR operation and the logic gate performing this operation is called NoR gate. A NOT gate followed by an OR gate makes a NOR gate. The basic logic construction of the NOR gate is shown below,



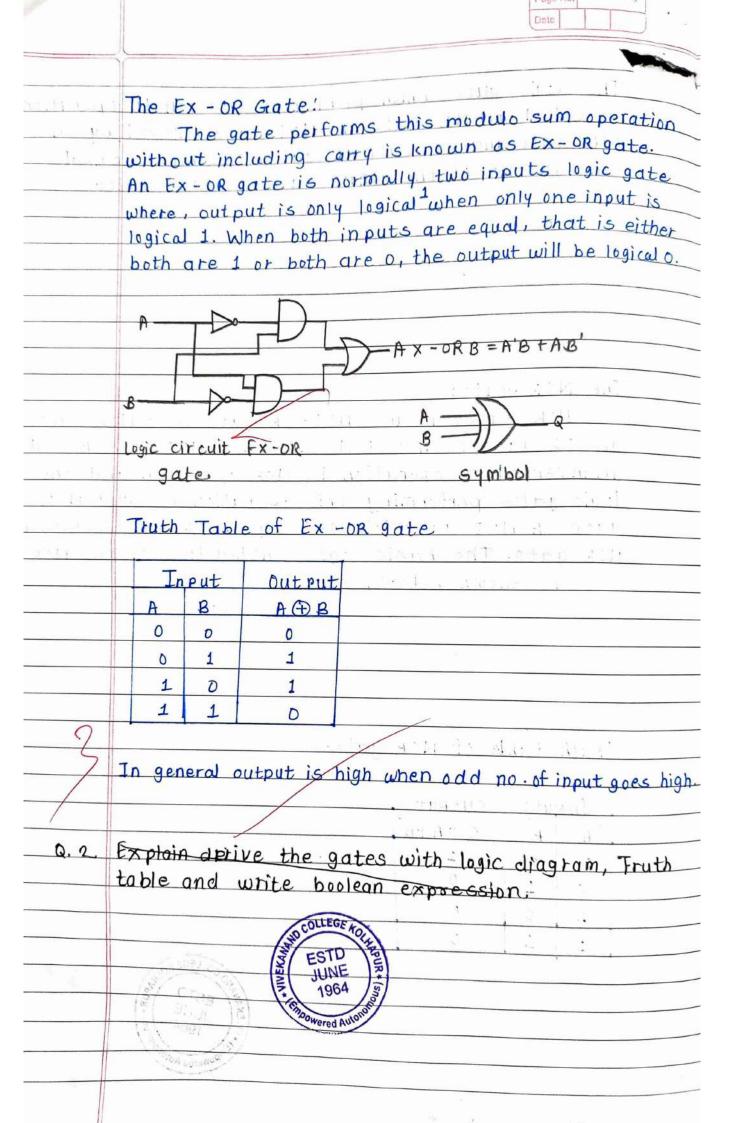
Logic circuit of NOR gate

symbol

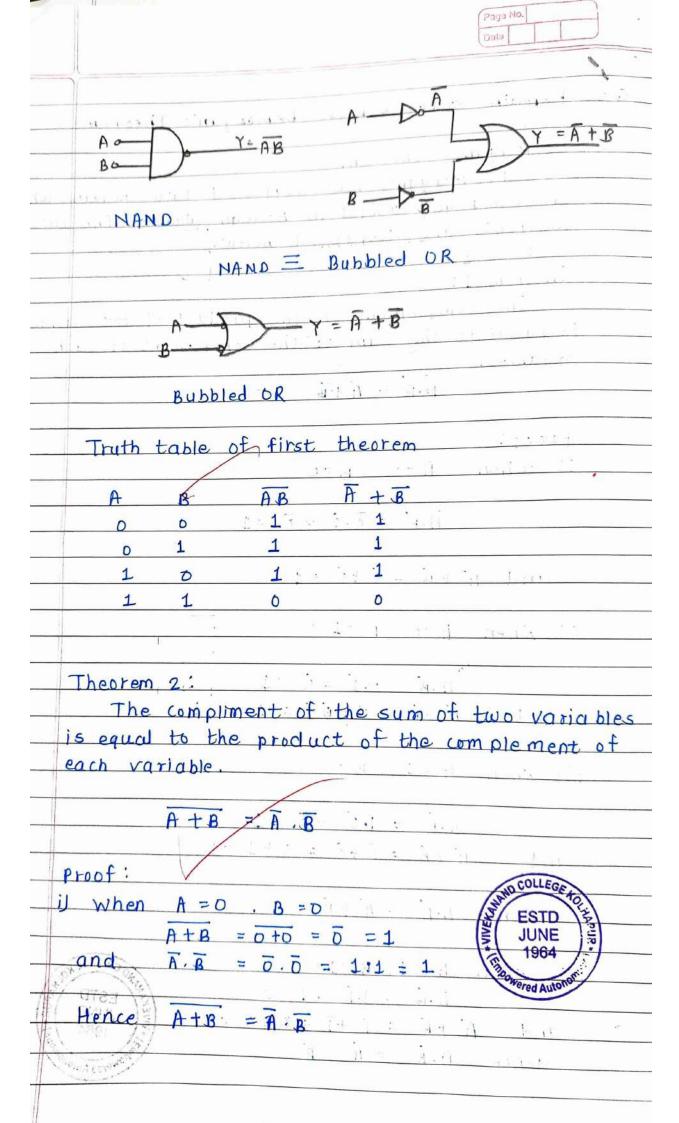
Truth table of NOR gate.

-11	-	F. To-		
	In	Puts	output	
	A	В	Q = A+B	
	. 0	100.	Sing 1 attice	enter out suitable distance of
	0	1	of Dogs	mortead stitue ber skint
	1	0	0	
	1	1	D	Street Control
1				127 GTan (2)





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When	A = 1, B = D
	A+B = 1+0 = 1 = 0
and	A.B = T. 0 = 0.1 = 0
Hence	$\overline{A} + \overline{B} = \overline{A} \cdot \overline{B}$

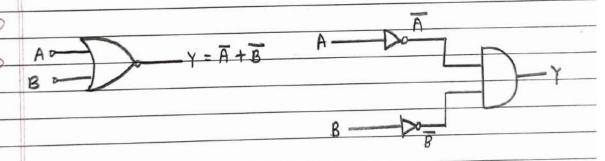
When
$$A = 1$$
, $B = 0$
 $A + B = 1 + 0 = 1 = 0$
 $A \cdot B = 1 \cdot 0 = 0 \cdot 1 = 0$
 $A + D = A \cdot B$

When
$$A = [B =]$$

$$\overline{A+B} = \overline{1} + \overline{1} = \overline{1} = 0$$

$$\overline{A} \cdot \overline{B} = \overline{1} \cdot \overline{1} = 0 \cdot 0 = 0$$
Hence, $\overline{A+B} = \overline{A+B} = \overline{A+B}$

Logic Diagram:



NOR = Bubbled AND



	Truth	table	of 2nd	Theorem
	A	В	A+B	A.B
1	0	D	1	1
1	D	1	0'	0
	1	0	b	0
	1	1	D	0



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	Assignmet Name = Vishwajeet Sub !- Electronic Roll No :- 7224. Std !- Bsc. FY.	Vija;	P			
Q.1. Explain Basic Gates with their logic diagrathruth table and wer write the bullian expression form. Their are three types of gates & OR, AND Not gates.					in	
	The OR Gate: - As its name implies, an OR. logic agate performs an OR, logic oper- ations, which is an addition. It has at kast two inputs. So, if A and B are its inputs, at the output we will find (A+B). so OR logic gate can be summarized by the formula Y= A+B-"If either A or B is true, then Q is true."					
	Ao	٠		table.		
	80	Inp	ruts	Output		
-	Symbol of OR	A	B	Q=A+B.		
- Jugor	TD RANGE TO THE PROPERTY OF TH	0	0	0		
L VEK	UNE R	0		1		
T.	ered Aurore	1/3	1	1		
DOW	ered Auton			,		
		As I	L 15 =	1000 1100		
	2] The AND Gate: - As it name implies can					

The AND Gate: - As it name implies an AND logic gate performs an "AND" logic operation, which is an multiplication. It has at least two inputs. So if A and B are its inputs, at the output we will find (AXB). So And logic gate can be summarized by the formula Y = AXB. "If both A and B are truth then Q is true"



Truth	table

1	Ae	Inputs		Output
1	p P	A	B	A.B.
	Symbol of AND	0	0	٥
	gate.	0	1	۵
	101 000 1000	·1	0	0.1.
	rational sections and section and	11.	(L. B. Late . Is a

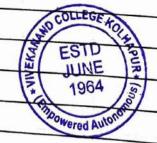
The Mot gate: As the name implies invertor the number entered. If you enter 'o' you will get a "1" on its output, and if you enter a "1" you will get a "o" on its output.

The inverter symbol is shown in given table.

Inverter gate is also known as Not and its output is V=A.

Truth table

	Output]
A	Q = Ā
0	1
1 -	0
	A 0 1



				DATE / /			
0.2.	Explain derived gates u	with th	reir l	logic diagr	am		
	truth table and write the bullian expression						
	form of it.						
	TI NIEWO O I I I I I I						
	The NAND Gate: 1- When output of an NAND						
	gate is inverted thro	gate is inverted through a NOT gate, the opena-					
	tion is called NAMD	opera	tion.	the logic	gate		
	which performs this NAND gate: A NOT &	vate 6	o page	d ha an A	unea_		
	gate makes NAMD &	acite. T	he ho	isic logica	1		
	construction of the	NAHD	aute	is shown	below.		
			7	2 2	22760		
			Truth	table.			
	A O AB	·		-	,		
	BO		puts	Output.			
	Ao	A	B	Q = AB'			
	B0 0 0	0	0				
	Symbols of NAND	0	0	1			
	gate.						
	dare		181				
2.	The NOR Gate :- N	OR 99	te me	ans Not	- 012		
	gate. In a NOR gate,	an o	R gat	e is inven	rted		
	through a NoT gate.	Actual	a an	inverted	OR		
-2	operation is NOR oper	ration	and	the logic	gate		
/	performing this opera	ation is	s calle	d NOR a	ite.		
	A NOT gate followed	by an	ORg	ate makes	s a		
-	NOR gate. The basic	logic	cor	struction	o F		
	the NOR gate is	Shown					
	Ac A+B		Irut	h table.	-		
	130	Inp	uts	Output	-		
	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$						
	A o	. 0	0	1 Jun CO	LLEGERO		
	80	0	(O SE ES	STD 3		
	Symbole of NOR	-1	0	101	964		
	Gare	1		O Bowered	Autonomo		



3	The Ex-OR gate !- The gate performs this
	modulo sum operations without including carry is known as Ex-or Gate. An Ex-or gate is
	is known as Ex- or Gate. An Ex-or gate is
	normally two inputs logic gate where, output
	is only logical 1 when only one input is logical
	1 when both inputs are equal, that is either
	both are 1 or both are on the output will
	be logical O.
	Truth table.

Symbol of ABABB

Ex-OR gate.

O O O O

I I

I O I



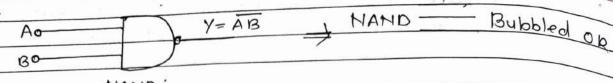
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3 1 6



-	
0.3.	State and proved Demorgan's Theorem.
	The complement of the product of two variables
	is equal to the sum of the comploment of
	$\frac{\overline{A} \cdot \overline{B}}{\overline{A} \cdot \overline{B}} = \overline{A} + \overline{B}$
	A.D - A 1 D
	·
	proof;
	(i) When A=0 1B=0
	A-B = 0.0 = 0 = 1
	and $\vec{A} + \vec{B} = \vec{O} + \vec{O} = + = $
	Hence, A.B = A+B.
	(ii) When A=0, B=1
	$\overline{A \cdot B} = \overline{0 \cdot 1} = \overline{0} = 1$
	and A+B = 0+T=1+0=1
	Hence, AB = A+B'
	bro = type the contract to
	Viii) When A=1 1B=0.
	$\overline{A \cdot B} = \overline{1 \cdot 0} = \overline{0} = 1$
	and $\vec{A} + \vec{B} = \vec{1} + \vec{0} = 0 + 1 + 1$
	Hence A·B = A + B.
	jy) When A = 1 , B=1
	$A \cdot B = 7.1 = 7 = 0$
	and A+B = 1 +1 = 0+0 = 0
	Hence A.B = A+B
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NAND.

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Truth table of first theorem

т					_
	A	13	AB	A+B	
	.6	0)	1	
	0	1	ľ		
	1	0	* [J	
	l l		0 .	0	
	1	/			7750

Theorem 2 and.

The complement of the sum of two variables is equal to the product of the complement of each variable.

A+B = A·B

proof :-

(i) When A=0 1B=0.

A+B = 0+0 = 0 =1

and A.B = 0-0 = 1.7 = 1.

Hence A+B = A-B

(ii) When A = 0 1 B=1

A+B = 0+1 = 0 T = 0 .

and A.B = 0-1 = 1.0 = 0.

Hence A+B = A.B

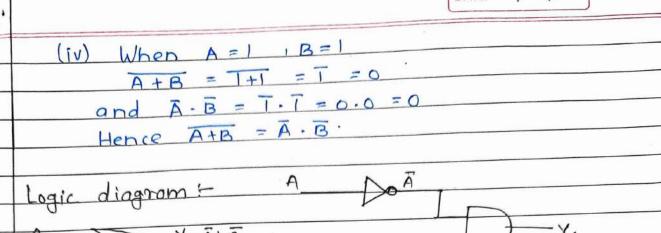
(iii) When A=1 1B=0

A+B = 1+0 = 1 = 0.

and A.B = 1+0 = 1 = 0

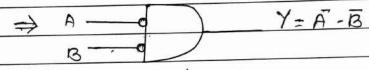
Hence, A+B = A.B





NOR B B

NOR __ Bubbled AND.

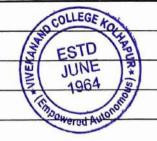


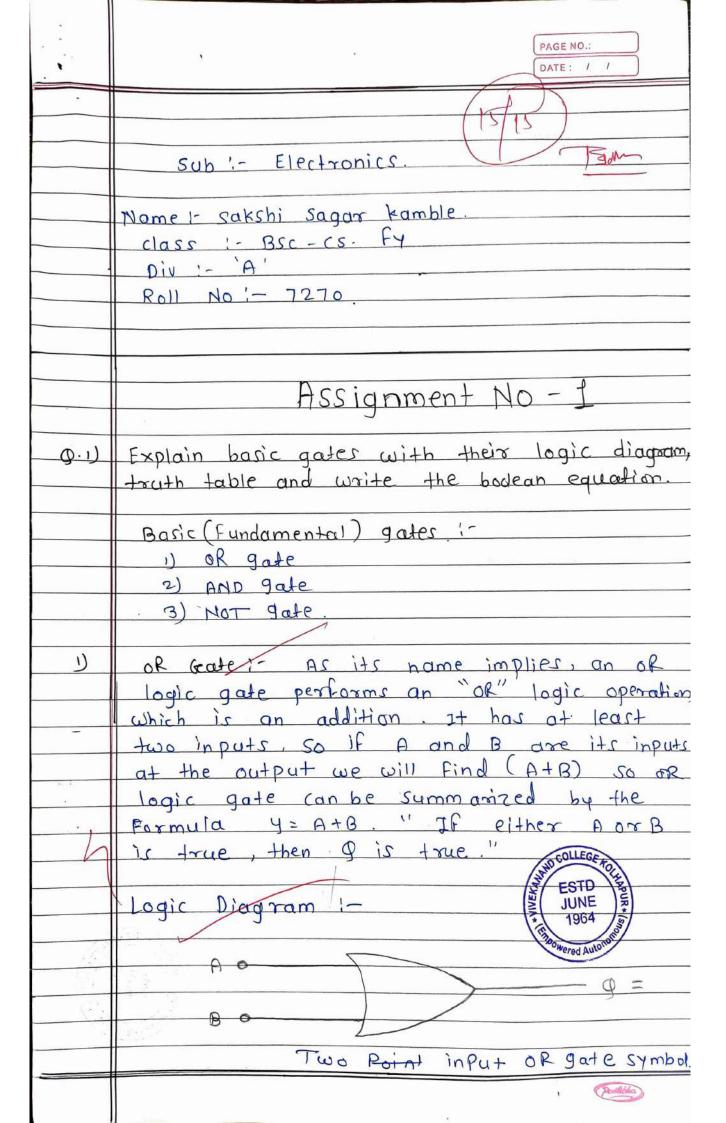
Bubbled AND

Truth table of gend Theorem

M. H. . . .

1						
	A	В	A+B	A.B.		
	0	0	1	1 4		
	0	1	0	0		
2	1	0	0	0		
	1	1	0	0 4		





	T	1.110 'C				
	Truth	Truth table :				
	Inp	out s	outputs			
	A '	В	9 = A + B			
	0	0	0			
	0	1	1			
	1	0				
	1	1	1			
	Truth	table of	or gate.			
	0 110		1			
	Boblea	n equation	- A + B.			
			H T D.			
3	AND GATE I - As it's name impiles					
		an AND logic gate performs an "AND"				
	logic operation, which is an multiplication It has at least two inputs so, if A					
	and B	one its	nputs, at the	00, 17 #		
	will	tind (AXB	1), 50 AND 1	odic aute		
	Can be	Summani	red by the F	Committee As 618		
	" fr bo	oth A and B	are true, +	hen g is		
	Logic Diagram!-					
	0					
(a)	<u>A</u>		1			
	7 77					
4	Two	input AND	gate Symbol.	NIVE KANA		
			gare symbol.	199		
				A mo		
				1964 (FIT D) * NOWN		

PAGE NO .: DATE: / / Truth Table 1inputs output Q = AB Truth table of AND gate NOT GATE !- As the name implies, invertor, will invert the number entered If you enter 'o", you will get a 'I" on it's output, and if you enter a "1", you will get a "o" on its output. The inverter symbol is shown in fig. 2.3. Inverter gate is also known as NOT and it output is 4= A. Logic Diagram !-Not gate symbol. Truth table ; Input output 9 - A Truth table of NOT Grate.

0

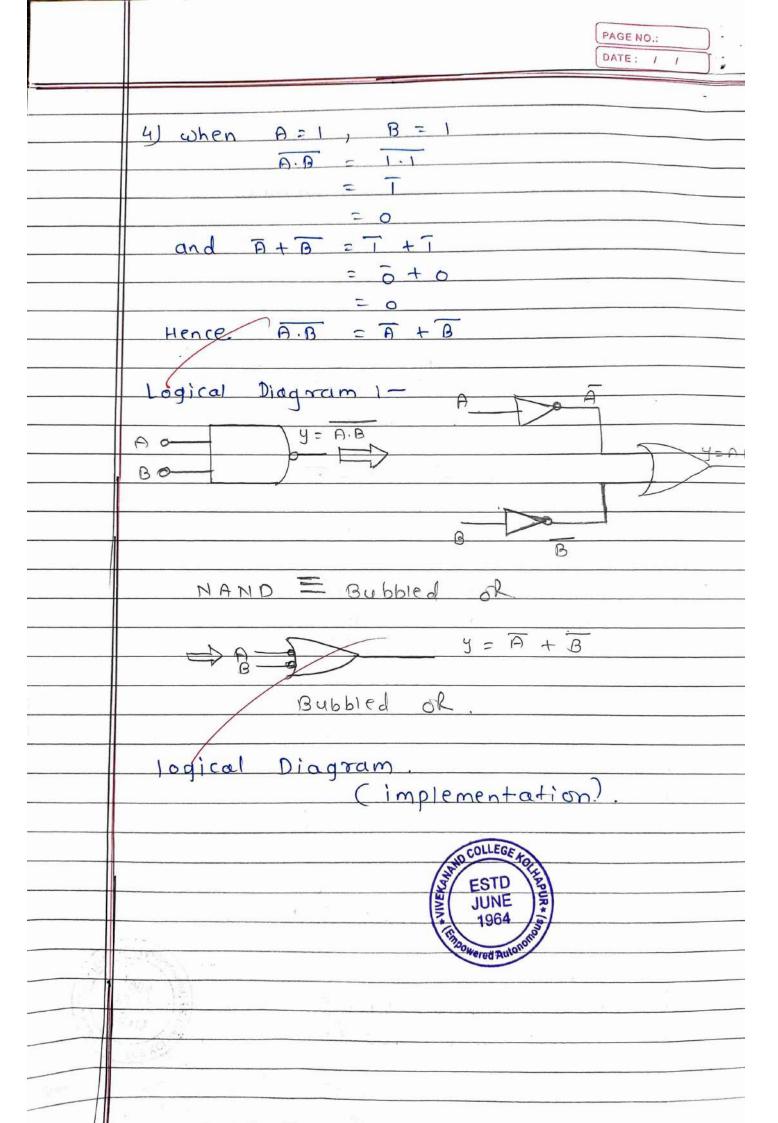
	PAGE NO.: DATE: / /
	Boolean equation !- y= A
0.2)	Explain derived gates with their logic diagram, truth table and write the boolean equation.
	Derived Gates. Derived Gates. Derived Gates. Nor gate NAND gate 3) Ex-or gate.
	Nor Gate: Nor gate means Not-or gate in it a q Nor gate, an or gate is inverted through a Not gate. Actually an inverted or operation is Nor operation and the logic gate performing this operation is called Nor gate. A Not gate followed by an or gate makes a Nor gate. The basic logic construction
7	of the NoR gate is shown below.
- 71	A - Q - A + B
The second	a) Togic circuit of NOR gate.
	b) Symbo), Sym

Postlóla

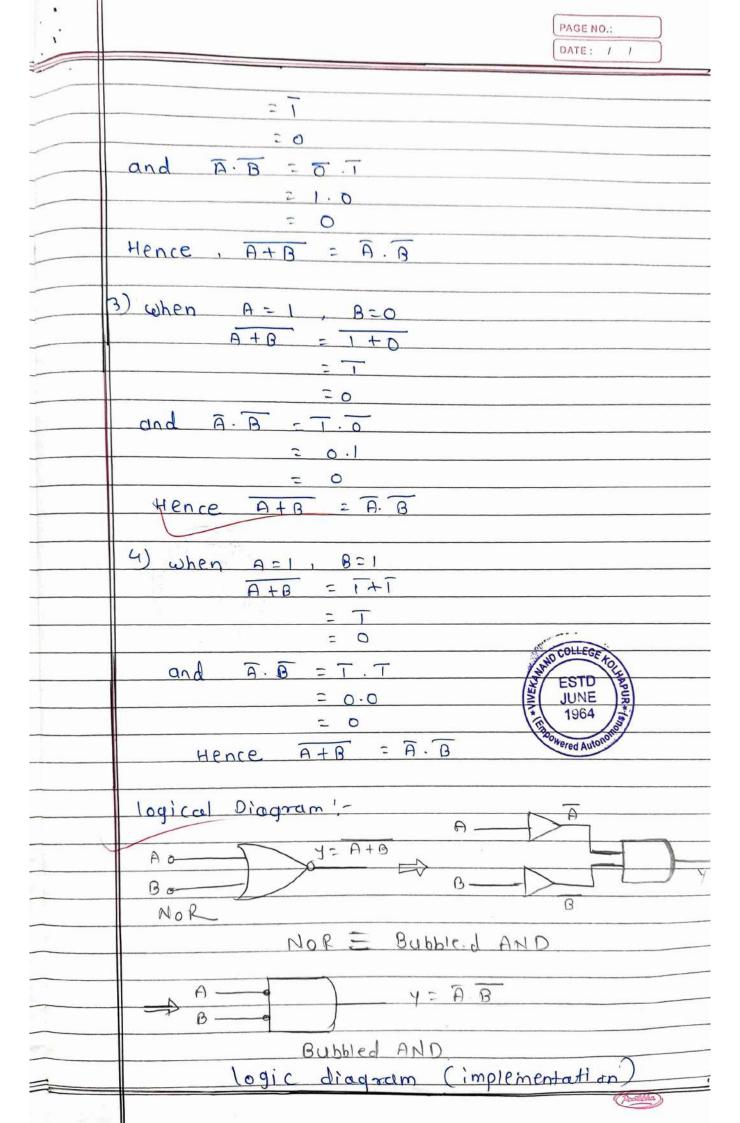
PAGE NO .: DATE: / / Truth table: output Inputs g = A·B 0 Touth Table of NAND gote Boolean equation: 7= A.B EX-OR GATE! - The gate performs this modul o sum operation without including carry is known as Ex-or gate. An logic gate where, output is only logical I when only one input is logical I when both inputs are equal, that is either both are I or both are or 0, the output will be logical o. logical Diagram 1-AX-ORB = AB + AB

PAGE NO.:

-	
	De Morgan's First Theorem i-
	Statement in The complement of the produc
	of two variables is equal to the sum of
	the complement of each variable.
	D.B = A+B
	proof = 1) when A = 0., B=0
	A.B = 0.0
	= 0
	and $\overline{A} + \overline{B} = \overline{D} + \overline{O}$
	= 1 +1
	= 1
X	
	Hence, A.B = A+B
	When A = 0, B=1
_	A.B = 0.1
	= 0
	_ = 1
	and A+B=0+1
	= 1 +0
	= 1
	Hence , A.B = A+B
	3) when A = 1, B=0
/	A.B = 1.0
	= D
	and the state of t
	AND B = 1 + D ST
	and D + 3 = 0 +1
-	= 1 TOTTE HOLD
-	
	Hence A.B = A+B

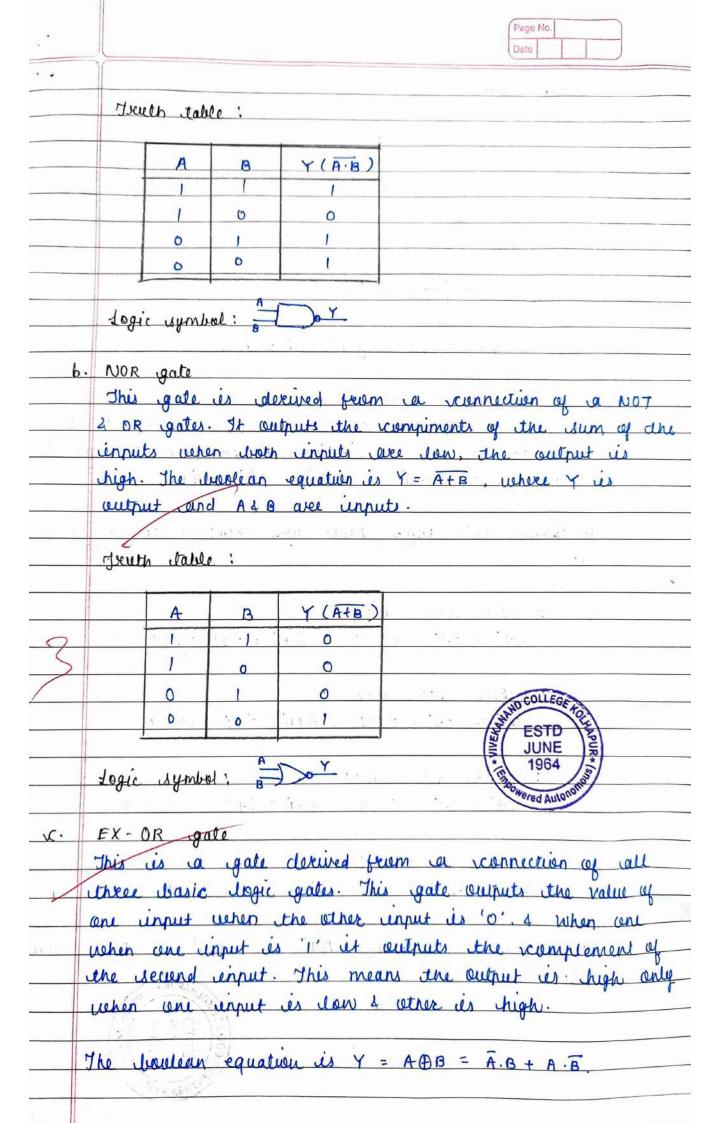


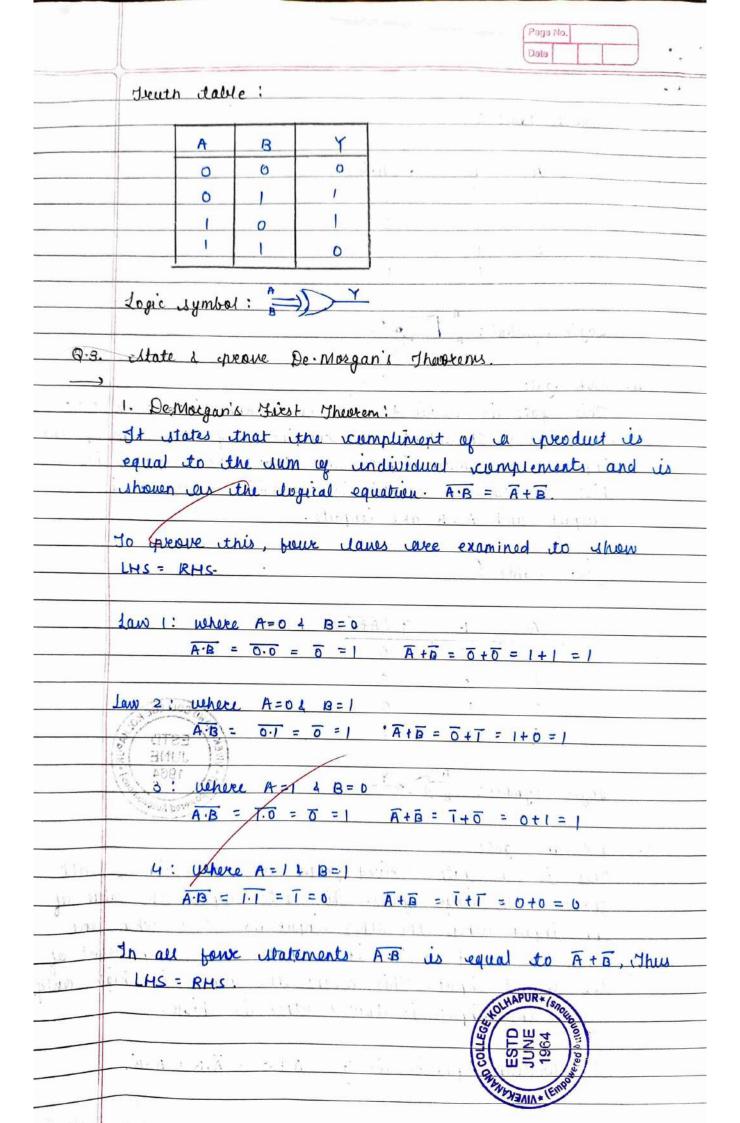
DATE: / Truth table ! Inputs output. Truth table of first Theorem. Bootean equation: A. Y = A + B · De - Morgan's second Theorem. statement: The complement of the sum of two variables is equal to the product of the Complement of each variable. A+B = A.B Proof !- 1 when A = 0, B=0 and A.B Hence A+B = A.B y when A=0, B=1



PAGE NO .: DATE: Truth Table 1-A + B A 0 0 0 0 0 0 0 Truth table of second Theorem. Boolean equation. = A.B. A+B Vered Auton

				seat No. BSc FY.		Page No.	
	Digital: Logic Gotes					13	
	Eightal. Lagic. gales						
٥.١٠	Explain basic gates with their dogic diagram, truth table						by toldo
	and boulean exp equation.						
		OR 90				1	
	Jh	is is	a basic	lugic gate	Inat	has two o	r mure
	unputs and only one output. The logic statement is						
	that when atteast one enput is high, the autput						
	uu	ll be	high. is	ince the or	gate	performs or	logic
1		ration				* 71 * 14 * 1	
- UANIX				ate Alegais and			
	Jh	2 bool		ituèn ils y (o			
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	Jh	L AND	gate o	operates on 1	he prei	inciple that	the
				only when			high
* 1/1			45.0	AND operal			
		Landy		5 Surpus II	1714	1.842 1.48	
1.11	Jho	L'ou	lean equ	cation is qui	ien by	y (output) =	A·B.
		where	L, AL	B are unput	. This	gate van he	we two
	02		unputs	•	• 100		
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	708	HC MAI	mbel: 4				
1			<u> </u>	****			
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·	Paga No.
	2. De Morgan's Second Theorem.
	It states that the complement of the sum of the
	two dinary digits is equal to the product of
	each oligits' romplement. And is shown by the given
	equation as $\overline{A} + \overline{B} = \overline{A} \cdot \overline{B}$.
	when A = 1 & B = 0
	$\overline{A+B} = \overline{A} \cdot \overline{B}$
	1+0 = 7.0
	T = 0·1
	0 = 0 LMS = RHS.
	when A=0 4 B=0
	AtB AB
	040 = 0.0
	∠ Þō=1.1
	1=1 : LHS = RHS
	When A& Bare
-1	A+B = A·B
	$\overline{1t1} = \overline{1.1}$
-	Ī = 0·0
	0 = 0 : LHS = RHS
	when A=0 + R=1

when A = 0 + B = 1 $A + B = \overline{A} \cdot \overline{B}$

0+1 = 0.1

T = 0.1

0 = 0 : LHS = RHS

