Vivekanand College, Kolhapur (Autonomous)
Department of Electronics
Notice

Date: 11.04.2023

All the students of B.Sc. I Electronics are hereby informed that their internal examination for Semester II will be conducted in offline mode as per attached schedule.

Paper	Section	Section title	Marks	Date	Time
DSC-1005B	I	Analog Electronics-II	15	24.04.2023	02:00 to 02:45 pm
	II	Digital Electronics-II	15	25.04.2023	01:00 to 01:45 pm

VIVEKANAND COLLEGE ESTD. JUNE 1964 KOLHAPUR-416 003

(Dr. C. B. Patil)
Head
Department of Electronics
Vivekanand College, Kolhapur.

Shri Swami Vivekanand Shikshan Sanstha's

Vivekanand College, Kolhapur (Autonomous)

Internal Examination (2022-23) Class: B.Sc.-I, Semester-II

Paper I: DSC-1005A Electronics — Date:-25/04/2023

Time: 1:00 pm to 1:45 pm — Marks: 15

Q. 1 Select correct alternative for the following: **[3 x 1 = 3]**

1. If an S-R latch has a 1 on the S input and a 0 on the R input the latch will be
   a) set b) reset c) invalid d) Clear
2. Flip flops are also called _____.
   a) Bi-stable dualvibrators b) Bi-stable transformer
   c) Bi-stable multivibrators d) Bi-stable singlevibrators
3. Positive edge-triggered flip-flop changes its state when _____.
   a) Low-to-high transition of clock b) High-to-low transition of clock
   c) Enable input (EN) is set d) Preset input (PRE) is set

Q2. Solve any THREE **[3 x 4 = 12 M]**

1. Explain working of RS Latch using NAND gates
2. Explain working of D flip-flop with suitable diagram
3. What is the role of preset and clear terminal of flip-flop with suitable example?
4. Explain working on T flip-flop with circuit diagram and truth-table
5. Explain the working of JK with circuit diagram and truth-table

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Shri Swami Vivekanand Shikshan Sanstha's

Vivekanand College, Kolhapur (Autonomous)

Internal Examination (2022-23) Class: B.Sc.-I, Semester-II

Paper I: DSC-1005A Electronics — Date:-25/04/2023

Time: 1:00 pm to 1:45 pm — Marks: 15

Q. 1 Select correct alternative for the following: **[3 x 1 = 3]**

4. If an S-R latch has a 1 on the S input and a 0 on the R input the latch will be
   a) set b) reset c) invalid d) Clear
5. Flip flops are also called _____.
   a) Bi-stable dualvibrators b) Bi-stable transformer
   c) Bi-stable multivibrators d) Bi-stable singlevibrators
6. Positive edge-triggered flip-flop changes its state when _____.
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Q2. Solve any THREE **[3 x 4 = 12 M]**

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10. Explain the working of JK with circuit diagram and truth-table

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Vedant Mangaonkar.

10/15

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– शिक्षणमहर्षी डॉ. बापूजी साळुंखे

08684

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VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

SUPPLIMENT

Signature of Supervisor	

Suppliment No. :

Roll No. : 7208

Class : BSI

Subject : Electronics II (Analog)

Test / Tutorial No. : Internal Examination

Div. :

Q1. i) In a transistor, $I_C = 10\ mA$ and $I_E = 10.2\ mA$ The value of β is 0.5

ii) c) positive as well as negative gate voltage

iii) c) V_P

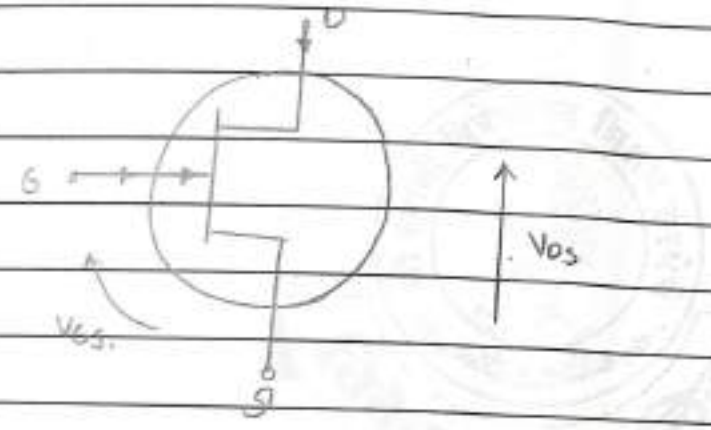
2

Q2. ii) N channel JFET :-

→ It JFET (junction feild effect transistor) is a three terminal semiconductor device in current is flowing through the ~~n~~ channel formed by n-type bar and PN junction.

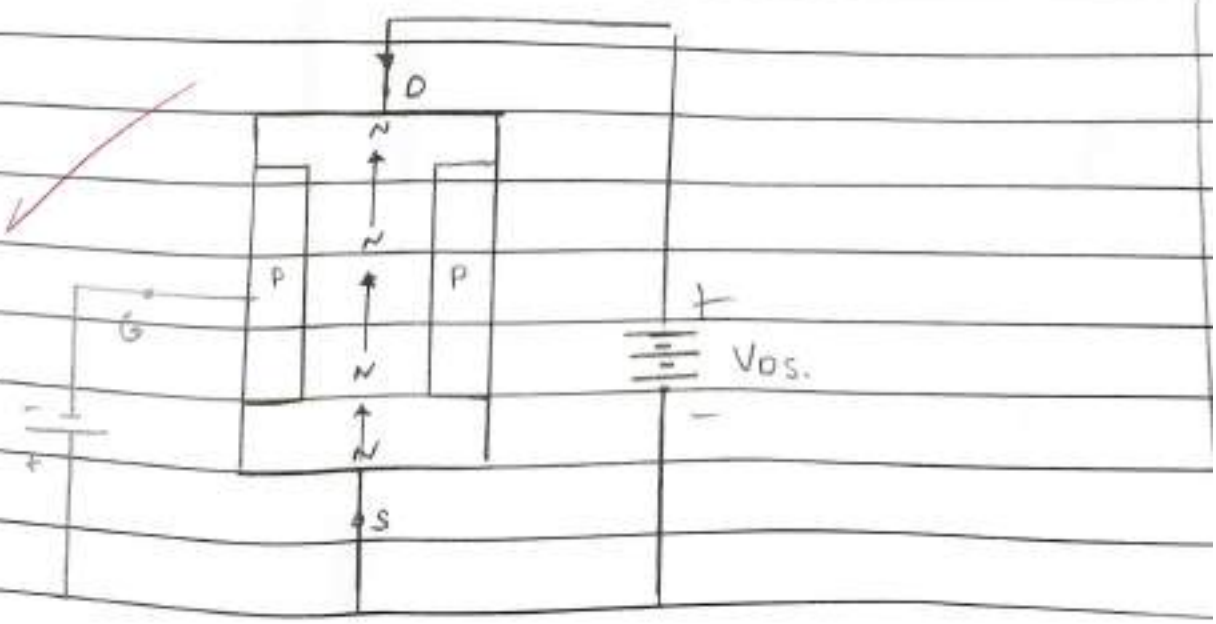
~~Construction :-~~

~~i) N-type material is used to form N type JFET JFET.~~



Symbol (N-channel JFET)

Working :-



i) in N channel JFET when Voltage is applied across Drain and source that forward voltage V_{DS} and reverge gate voltage V_{GS} kept '0' the deplection region is ~~formed on~~ established and the drain current I_D flows from D to S through the channel.

ii) When we apply positive reverse voltage V_{GS} on gate terminal of JFET is reverse biased the size of the depletion layer formed moreases which leads to narrowing of the channel and causes ~~less~~ narrow channel for conduction which results in less current I_D through the JFET.

iii) as we continue increasing the reverse voltage at certain stage the depletion layers increases so that no ~~spe~~ space of carriers left which resulits in no current flowing through the JFET
This voltage is called as $V_{GS(OFF)}$

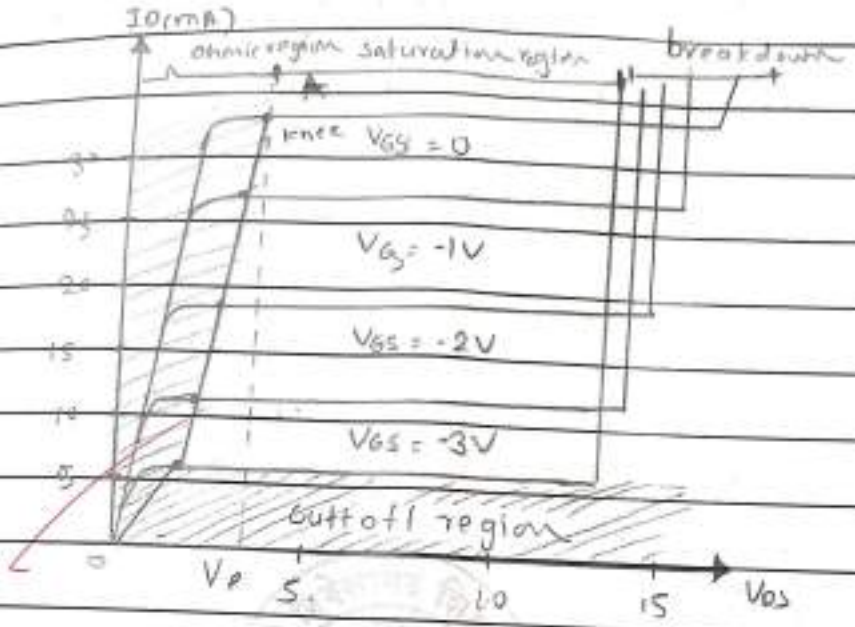
iv) When we apply negative reverse voltage ~~a~~ to gate terminal. the depletion layer formed start decreasing thus the channel get wide and more current flows through it.

v) at certain voltage V_{as} the drain current becomes constant known as Pinchoff voltage (V_p)

vi) when ~~max~~ $V_{GS} = 0$ ~~it~~ maximum drain current flows through the JFET i.e. I_{DSS}.

Drain Characteristics :-

The graph between V_{DS} and I_D is called as Drain characteristics.



The Drain characteristics is divided in 3 regions

i) ohmic 2) ~~sto~~ saturation region 3) breakdown region

1) Ohmic region. → In ohmic region. we can see that the current I_D increases with increase in output voltage V_D.

The region on left of the curve OA is ohmic region.

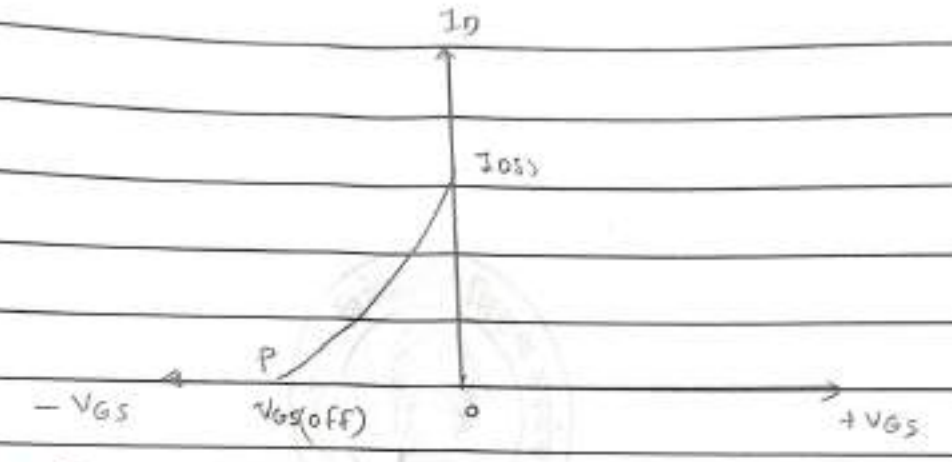
in this region it obeys ohm's law as it acts as simple resistor.

in this region source gate are shorted

ii) Saturation region :- after V_P there is very less gap to ~~trabel~~ ~~ehe~~ current to flow. so the current I_D becomes constant in saturation region as V_{GS} goes increasing the certain ~~Voo~~ the ~~current~~ the ~~je~~ JFET undergoes cutoff ~~re~~ V_{GS} condition.

iii) break down region :- at maximum V_{DD} at certain V_{GS} a very large current flows through the JFET which causes breakdown of JFET, as at $V_{D(max)}$ the current suddenly rises at its max.

Transfer characteristics :



1) as we can see at $V_{GS} = 0$ the current I_D is max that I_{DSS}.
2) - negative voltage V_{GS} increase at point the current I_D becomes zero.
3) the JFET is safely operated from 0 to $V_{GS(OFF)}$

Name:- Omkar Sunil misal

7/15 8

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SUPPLIMENT

Signature of Supervisor	

Suppliment No. : 1
Roll No. : 7209
Class : BSC-FY

Subject : Analog electronics -II
Test / Tutorial No. : Internal examination
Div. : A

Q.1 # MCQ

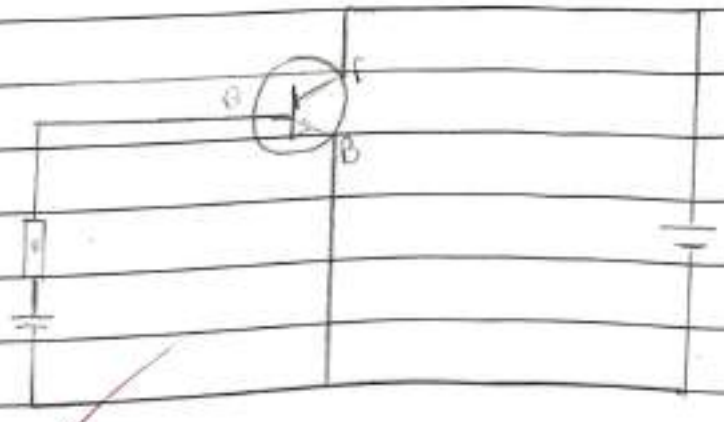
i) In a transistor, $I_C = 10mA$ & $I_E = 10.2mA$. The value of β is 0.5

ii) A ~~Prof~~ MOSFET can be operated with c) Positive as well as negative gate voltage

iii) For $V_{CE} = 0V$, the drain current becomes constant when V_{DS} exceeds c) V_P

Q.3. i) Explain DC load & Q-point.

→



Consider a circuit which does not have any input the voltage +Vcc is a input is called as quintial condition.

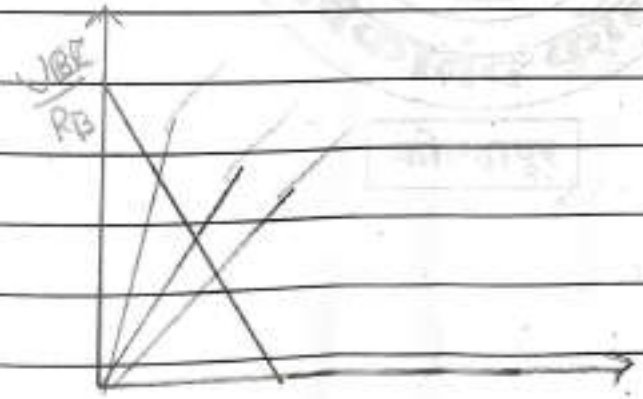
Applying kirchhoff's voltage law.

$V_{CC} = I_C I_E + V_{BE}$

Rearranging in eqn, for I_C

$$I_C = \left(\frac{1}{R_C}\right) I_B + \left(\frac{V_{CC}}{R_B}\right)$$

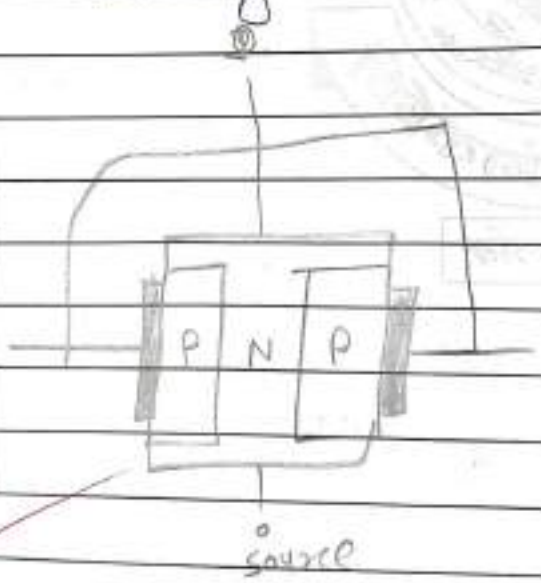
The eqn is look like $y = mx + c$ when the

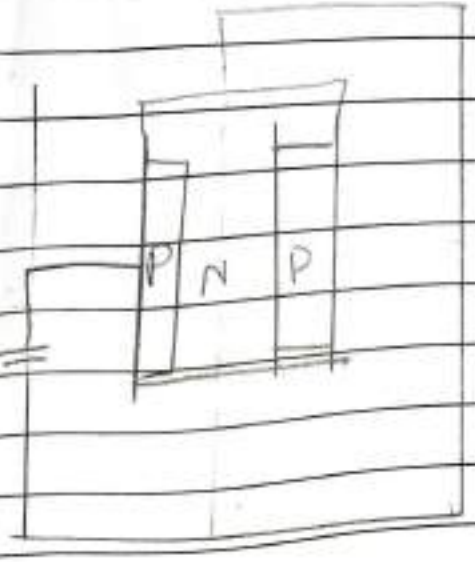


2. ii) N channel JFET

→ A JFET (junction field effect transister) is a three terminal semiconductor device in current is flowing through the channel formed by n-type bar and p-N Junction

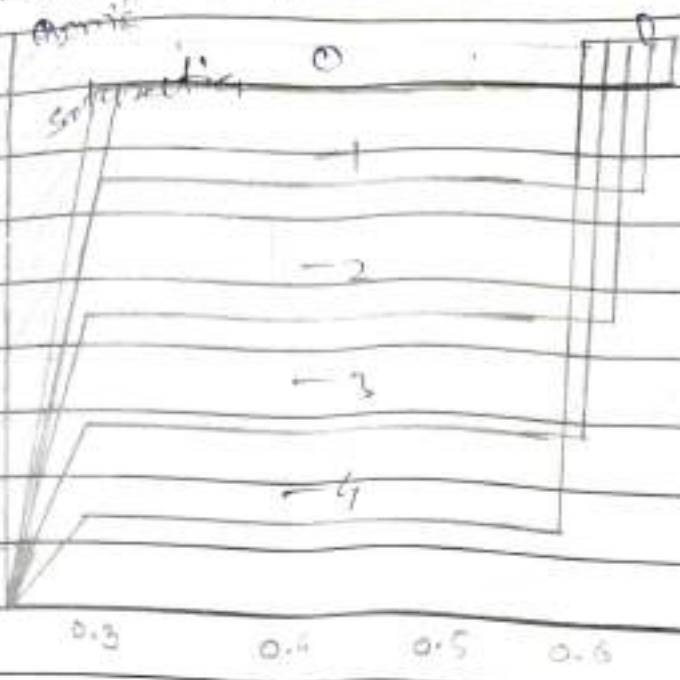
Working.





3

Drain characteristics



The drain characteristics is divided in region:

1) Ohmic. 2) Saturated region Breakage region

Ohmic region :- In ohmic region are increase in output

The region on the left on the current is called ohmic region

In this region it obeys ohm's law as it acts as simple resister.

ii) Saturation region :- After up there is a very Can gap to current to flow

So the current I_D becomes constant in Saturation region as vgs goes increasing the certain the FET Undergoes cut of was condition

n' n channel JFET when voltage & when voltage Drain and Source that formly voltage is applied across Drain & Source that forward voltage VDS and reverse and it

Zahir Jamir Mujawar

9+2=11/15 (B)

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VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

08987

SUPPLIMENT

Signature of Supervisor	

Suppliment No. :

Roll No. : 7210

Class : BSC-I

Subject : Electronics-2

Test / Tutorial No. : Internal examination

Div. : C

Q1]

1]

a) 0.2

2)

c) positive as well as negative voltage

3) c) Up

2

Q.7

(1)

If CE configuration input current I_B and Input voltage V_{CB} at constant output voltage V_{CC} is called as input characteristic

$$\therefore CE = \left.\frac{I_B}{V_{CB}}\right|_{\text{const} = V_{CE}}$$

∴ Input current I_B and Input voltage V_{CB} at const. output voltage V_{CC}. In group the value of V_{CE} is slightly less when $I_B = 0$

* Output Characteristics

↳ In output Characteristics output current region

$\therefore CC = \frac{IC}{VCE}$ | constant

In output characteristics Vs reverse method of input characteristics their are three parts.

(i) Active region (ii) Cut-off region
(iii) Saturation region

(i) Active region-

In active region output current by output voltage at const input current

$\frac{Ic}{VCE}$ | at cont $= I_B$

value of Vce is increasing while increasing of output current at constant input current $I_B = 0$

(ii) Cut-off region.

If $I_B = 0$ then value are in cut-off region mean no value in this region

(iii) saturation region

In saturation region the values the values are increasing this is ohmic region

(2) Equivalent circuit of UJT.

the equal equivalent circuit of UJT terminal base B_1 and base B_2 and emmiter open is known as inter-base resistance

Therefore- $R_B = R_{B_1} + R_{B_2}$

Where, R_{BB} = inter-base resistance
R_{B_1} = termind resistance both R_{B_1} and emitter
R_{B_2} = termind resistance both R_{B_2} and emitter emitter

In this ~~character~~ circuit when P-type material applied on n-type material.

∴ R_{BT} = is always greater R_{B1} with emitter

- The battery V_{BB} is on current base throughout
- The value of R_1 means V_c is

$$V_c = \left[\frac{R_{B1}}{R_{B1}+R_{B2}}\right] V_{BB}$$

$$V_c = \eta V_{BB}$$

∴ The η is stand off and its value is

$$\eta = \left[\frac{R_{B1}}{R_{B2}+R_{B1}}\right]$$

Siddharth. Deepak Nesarkar

6+1=7
15

08965

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Shri Swami Vivekanand Shikshan Sanstha Kolhapur's

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SUPPLIMENT

Signature of Supervisor

Suppliment No. :

Roll No. : 7211

Class : BSC-I FY

Subject : Analog electronics II

Test / Tutorial No. : Internal Exam

Div. : A

Q1. Select Correct alternative

1] Y → A

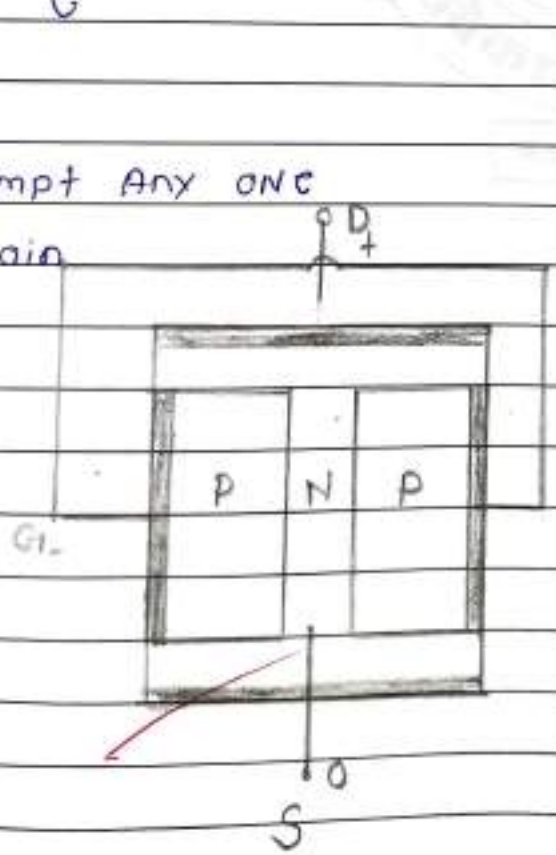
2] → C

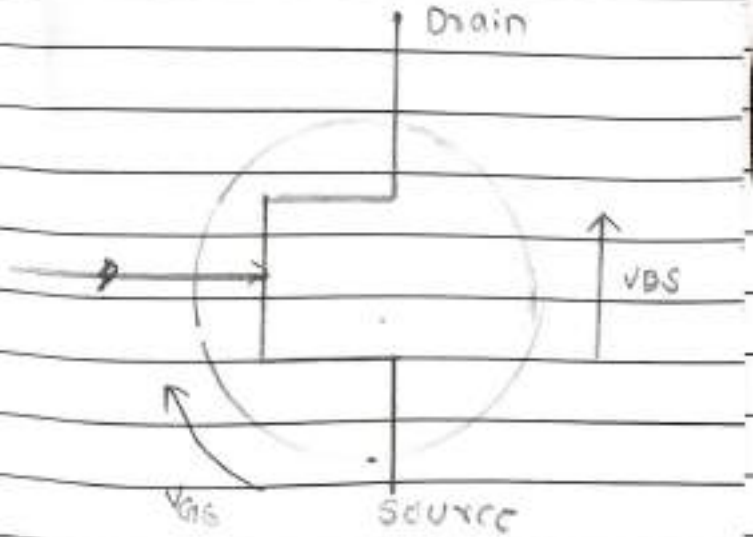
3 → G

4]

Q2. Attempt Any ONE

2] Explain

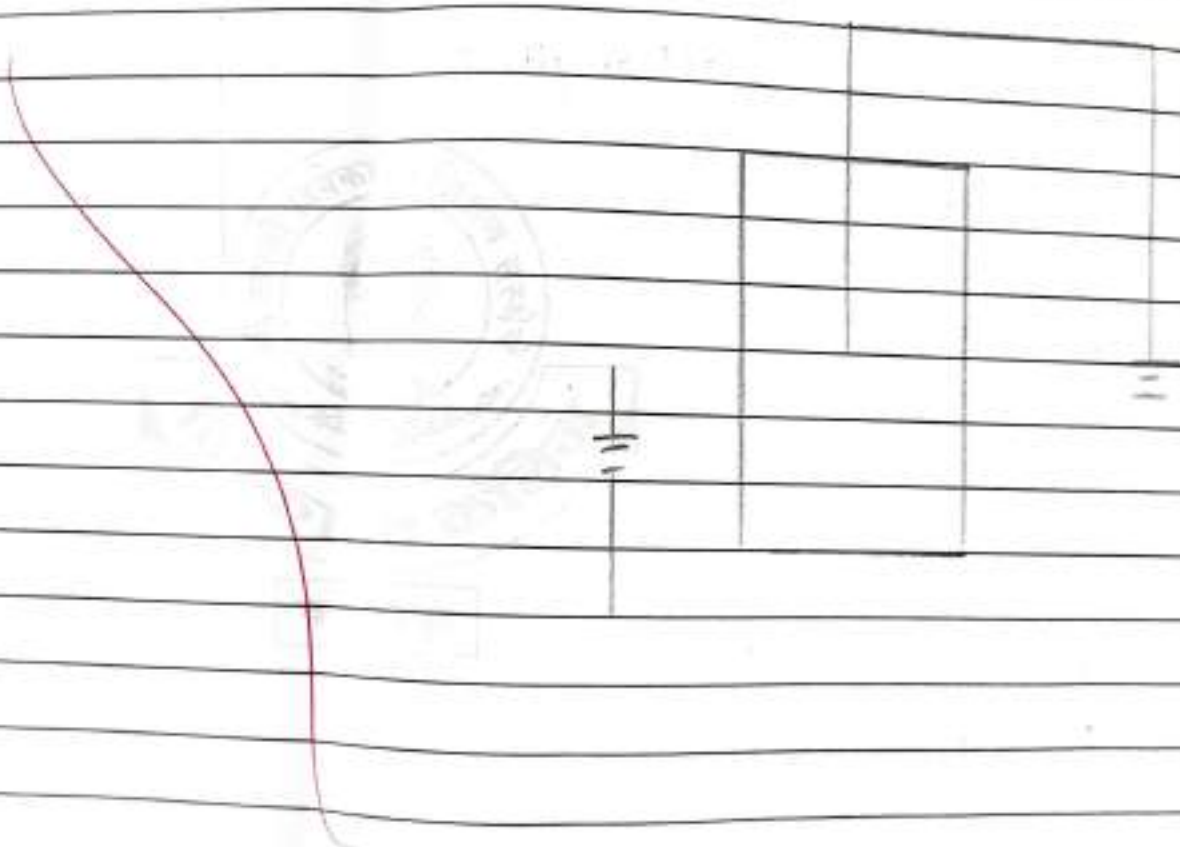




1) A junction field effect transistor is a three terminal semiconductor devices in which current conduction is by an type of carries.

2) A JFET consists of a n-type current passes through consists the bar forms the conducting channel for the charge carries. If the bar is type it is called as n-channel JFET.

3) The JFET has high Input impedance and low noice level.



Q3 2)

→ The equivalent circuit of UJT is shown in the resistance between terminal Base 1 and Base 2 with emitter open is called inter base resistance (R_{BB})

$R_{BB} = R_{B1} + R_{B2}$

where, R_{BB} = inter base resistance.

R_{B1} = Resistance between terminal Base 1 and emitter

R_{B2} = Resistance between terminal Base 2 and emitter.

The volume of inter Base resistance lies in the range of 4.7 kΩ to 10 kΩ. The value R_{B1} and R_{B2} depends on whether p-type material.

Name :- Sujal . K. Vyavahare

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08995

Shri Swami Vivekanand Shikshan Sanstha Kolhapur's

VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

SUPPLIMENT

Signature of Supervisor	

Suppliment No. : 1
Roll No. : 7222
Class : BSC-I

Subject : Analog Electronics-II
Test / Tutorial No. : Internal Exam
Div. : C

Q.1 Select Correct Alternatives.

(i)

→ B) 0.5

(ii)

→ C) Positive as well as negative gate Voltage

(iii)

→ C) V_p

Q. 2

(1)

→ If Configuration Common emitter Configuration below. is the diagram Which is the show the characteristic of the CE Configuration. The diagram is arrangement of for input and output characteristic.

Output characteristic :-

The graph of the output voltage and output current of Constant current is called output charac. From the above graph we can these are 3 region a graph neatly (a) saturation region (b) active regation (c) cut off.

b) Active region :- When the Collector Current increases then is increase

Q. 3

(ii)

→ The equivalent circuit of UJT is show in the figure. The resistance between the terminal, Base 1 ent base 2 with the emitter. Open is called as the interbase resistance (R_{BB}).

$$R_{BB} = R_{B1} + R_{B2}$$

When,

R_{BB} = Inter Base Resistance

R_{B1} = Resistance bet, terminal base & emitter

R_{B2} = Resistance bet, terminal base and R_B

The Value of interbase resistance lies in the range of 4.7Ω to 10Ω to the Value of R_B, & R_B depends upon the P type material is located ds along the n type bar material.

As the emitter (e) is located close to base 2 termin the resistance R_1 greater than resistance R_2

• The greater

08/15 Roll no - 7313 , Name - Patil Sourabh Bhagawan , class - Bscfy .

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08941

Shri Swami Vivekanand Shikshan Sanstha Kolhapur's

VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

SUPPLIMENT

Signature of Supervisor	

Suppliment No. :

Roll No. : 7313

Class : Bsc.Fy

Subject : Electronics Ditital

Test / Tutorial No. :

Div. : A

Q.1.

1.

→ a) set

2)

→ c) Bi-stable multivibrators

c 3

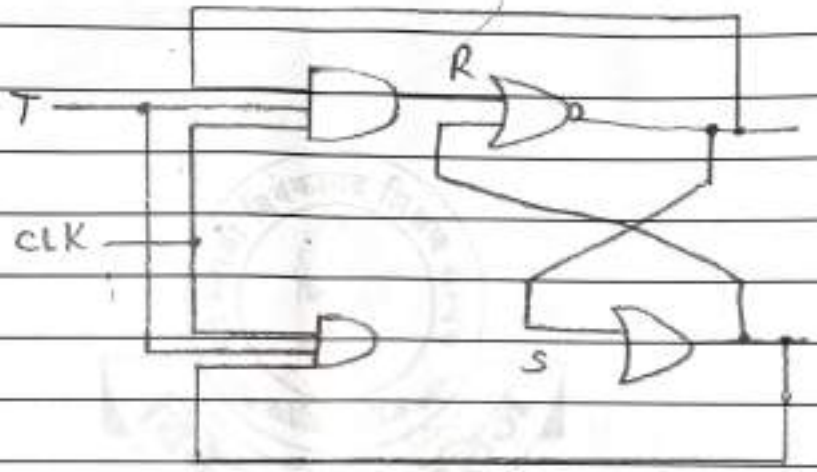
3)

→ a) Low-to-high transition of clock

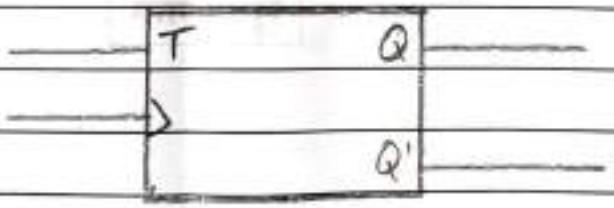
4)

→ T flip-flop - 1) T flip is a single input logic circuit that holds or toggles its output according to the input state. Toggling means changing the next state output to complement the current state. T is an abbreviation for toggle.

2) A good example to explain this concept is using a light switch



Logic Diagram



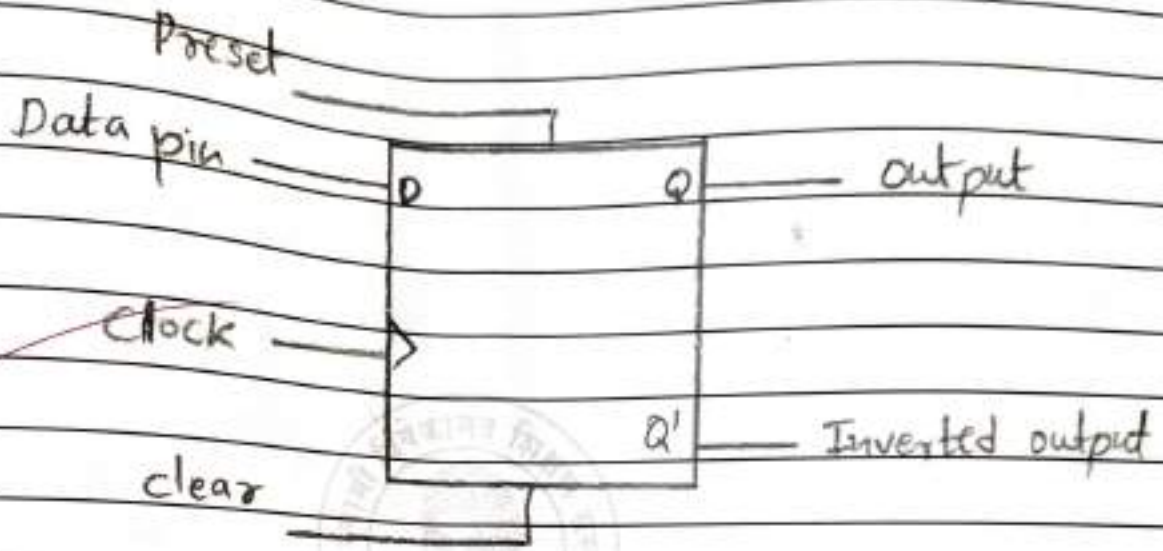
Symbol

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

table

3)

→ D flip flop - 1) The D flip flop has only two inputs D and CP. The D inputs go precisely to the S input and its complement is used to the R input. Considering the pulse input is at 0, the



Symbol : D flip flop

08/15 Harsh Nivas Yadav

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VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

SUPPLIMENT

Signature of Supervisor:

Suppliment No. : 1
Roll No. : 7224
Class : BSC I

Subject : Electronics II
Test / Tutorial No. : Enternal exam.
Div. : A.

Q.1 ① a) set

② b) Bi - stable transformer

③ a) Low - to high transition of clock.

1.2 ①

RS Latch using NOR/NAND gate:-

① Block diagram

② Circuit diagram.

③ Truth table

Input		output		Action
S	R	Q	$\overline{Q}$	
0	0	last state	last state	No change
0	1	0	1	Reset
1	0	1	0	set
1	1	0 (forbidden)	0 (forbidden)	forbidden

④ Working:-

RS flip flop using NOR can be constructed as shown in diagram in which output of one gate is given to input of other gate.

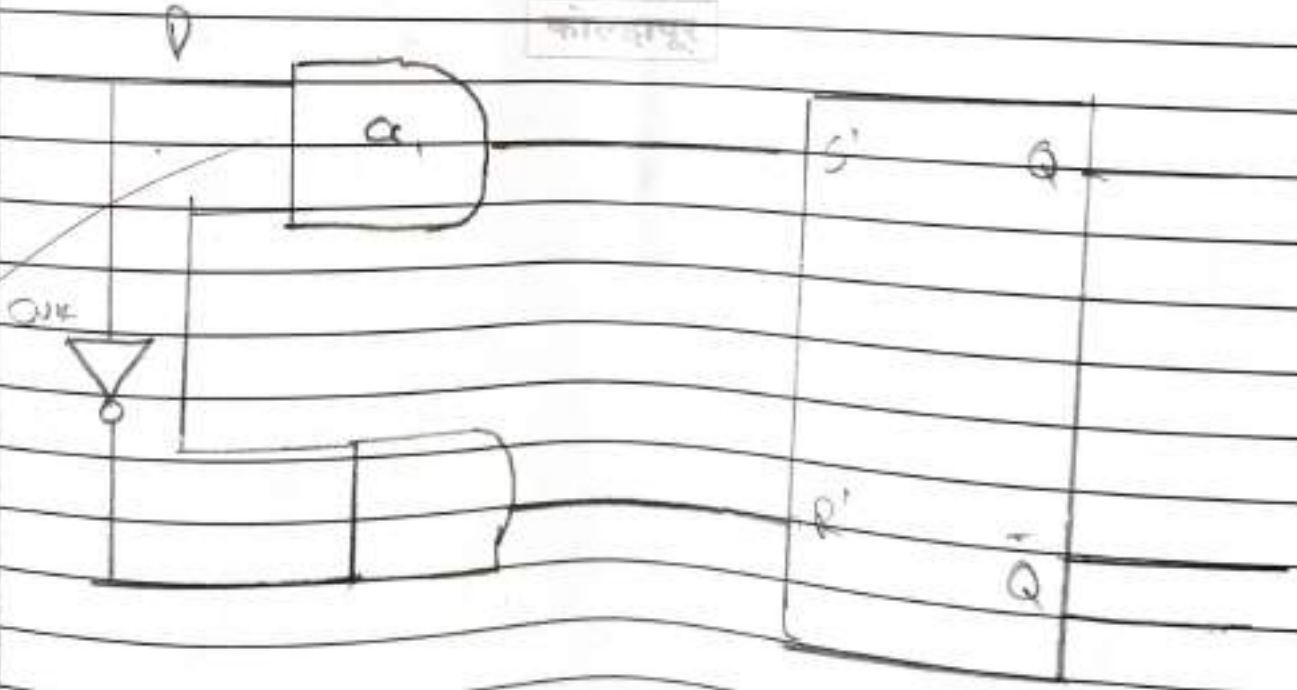
In case of NOR gate if one of the input is high then output becomes low.

case I :- when S = 0 , R = 0

when there is 0 at the input of the NOR it do not have any effect on the output so output remains in the state
If o/p Q = 1 and $\bar{Q}$ = 0 the input to FF are R = 0 , S = 0 then o/p remains in the state last Q = 1

case II :- when R = 1 , S = 0
when Q = 0 R = 1 the o/p of G, i.e Q = 0 it cause $\bar{Q}$ = 1 the condition Q = 0 is called as resting the flip-flop.

(2) circuit diagram :-



CLK	D	Q_{n+1}	Action
0	x	last state	No change
1	0	0	Reset
1	1	1	Set

② Truth table.

11½ = 12/75

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09082

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SUPPLIMENT

Signature of Supervisor

Suppliment No. :

Roll No. : 7208

Class : BSc I. sem II

Subject : Digital Electronics II

Test / Tutorial No. : Internal examination

Div. :

Q 1.

1. a) set

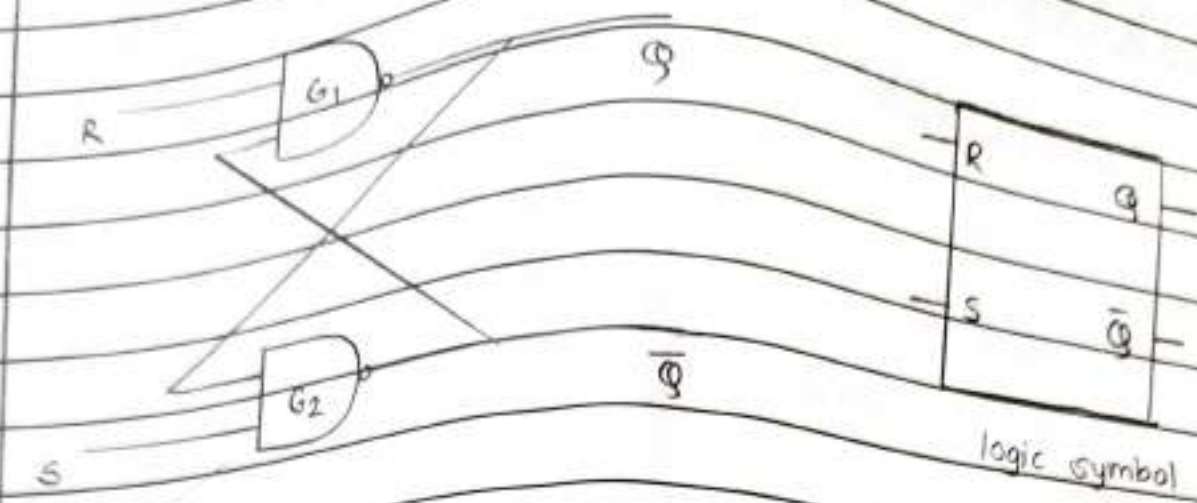
2. c) bistable multivibrator.

3. a) low to high transition of a clock.

03

Q2.

1. RS latch using NAND



logic diagram.

logic symbol

Inputs		Output	action.
R	S		
0	0	forbidden ~~St.~~	No change
0	1	1	set
1	0	0	reset
1	1	last state	no change.

Truth Table

RS latch using NAND gates is consisting of two NAND gates G_1 and G_2 where ~~out~~ feedback of G_1 is as input of G_2 and feedback of G_2 is as input of G_1 For NAND if any input is low output is high

Working:

Working of RS latch depends on inputs given to R and S. which can be studied by using following 4 cases

Case I :- R = 0 and S = 0

when R=0 and S=0 both gates G_1 and G_2 are ~~dis~~ outputs become 1 i.e $Q = \bar{Q}$

which is not possible i.e. it is called a forbidden state and there is no change in output

Case II, R = 0 , S = 1

as input R becomes zero the gate G_1 is enabled and G_2 is disabled ∴ we can see $Q = 1$ and $\bar{Q} = 0$ ∴ output is 1 and the flipflop is in set condition.

Case III, R = 1 , S = 0

~~as input S becomes 0 one the G2 is disabled~~

as input S becomes 0 the gate G_2 is enabled and output $\bar{Q} = 01$, ∴ gate G_1 is disabled and output $Q = 0$ ∴ flipflop is in reset condition

Case IV : R = 01 S = 01

for R = S = 01 both gates are disabled so there is no change in output and the flipflop remains in last state

~~Q2~~

Q2

3. Preset and Clear :-

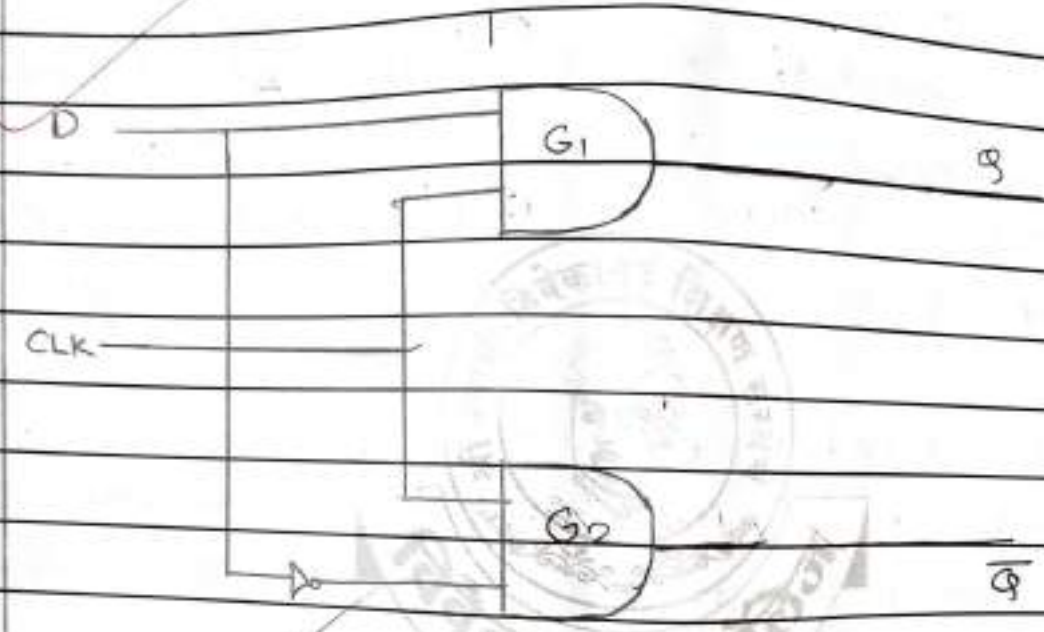
In a flipflop ~~we n~~ if neccesary we give additional input to ~~ff~~ circuit after the latch or the ~~flipflop~~ gate ~~inputs~~ using OR gate.

This is used to eleminate the action of flipflop on further circuit in ncessary conditions.

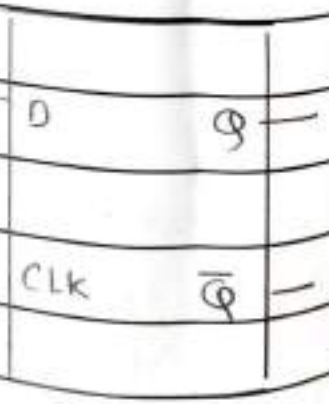
82.

2. D flipFlop :-

D flipflop is constructed by using ~~RS flipflop~~ but both inputs are from same input source D the only difference is it is connected to second gate using ~~Not~~ inverter (NOT) gate. as shown in fig. and clock pulse is given



logic Diagram



logic symbol.

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Subject :

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Div. :

2.2.

CLK	D	output	Action
0	X	X	last state
1	1	1	set
1	0	0	reset.

working :-

working of D flipflop depends on both clock pulse and input D.

when CLK = 0 the flipflop is independant of input that is it is under dont care condition

case I. :- when CLK = 1 and D = 1

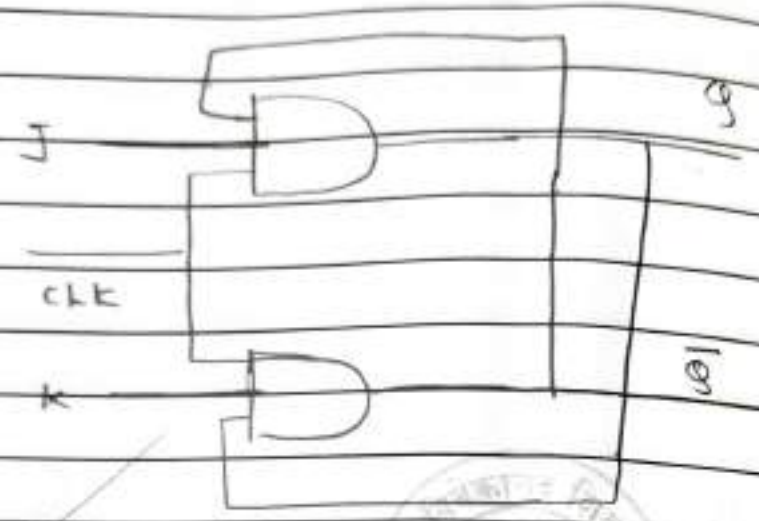
when D = 1 the gate G_1 is enabled and the output Q becomes 1 thus the flip flop is said to be under set state.

case II :- when CLK = 1 and D = 0

when D = 0 the gate G_1 is disabled but the gate G_2 is enabled as it is connected using inverter gate $\therefore \bar{Q} = 1$ and $Q = 0$

∴ The flipflop undergoes reset condition.

12 (a) ~~T flipflop~~. JK flip flop.



circuit diagram.

Roonam Narsu Patil

$11\frac{1}{2} = 12/15$

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Test / Tutorial No. : Internal Exam

Div. : A

0 1]

1] a] set

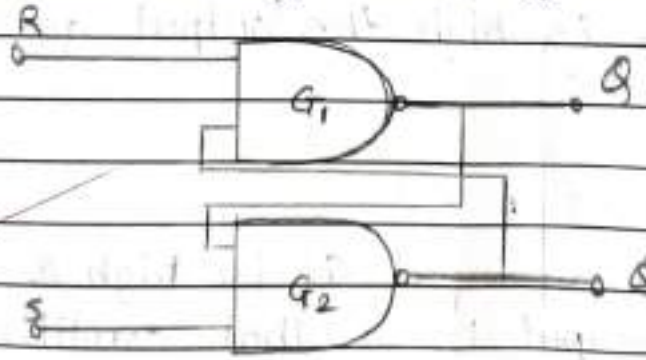
2] c] Bi-stable multivibrators

3] a] Low-to-high transition of clock

Q 2]

1]

→ RS Latch useing NAND gate



• circuit Diagram of RS NAND gate

• Logic symbol

Tauth-Table

I/P.		O/P	
R	S	Q_{n+1}	action
0	0	Q_n	LS (No change)
0	1	1	set
1	0	0	reset
1	1	FB	Race

04

Working:

case I: R = S = 0

When the both input are low the output is in last state.

case II: R = 0, S = 1

When the ~~one it~~ upper input is G_1 is low & lower input G_2 is high the output goes in ~~last~~ setting state.

case III: R = 1, S = 0

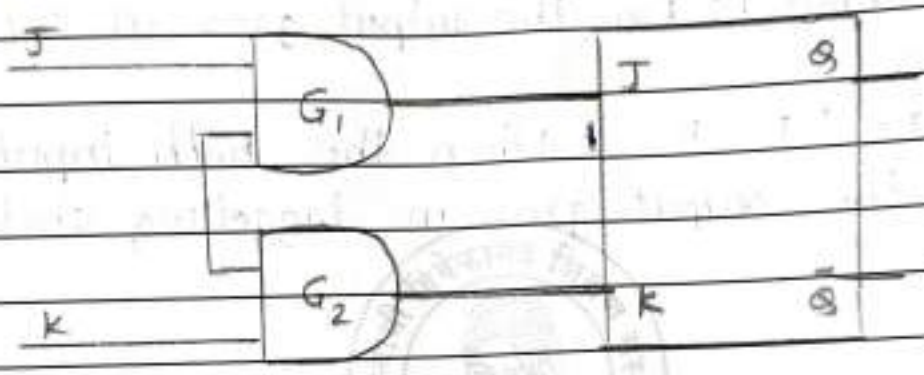
When the upper input G_1 is high & lower input is low the output is 0 that condition is called resetting the flip-flop.

case IV = R = S = 1

When both input are high the output goes in forbidden condition.

5]

→ JK flip-flop



• Circuit Diagram

• Logic Symbol

Tauth-Table

Inputs		outputs
J	K	Q_{n+1}
0	0	Q_n (LS)
0	1	0
1	0	1
1	1	$\bar{Q}_n$ (Toggle)

Working:

case I : J = K = 0 When the both inputs are low the output goes in last state.

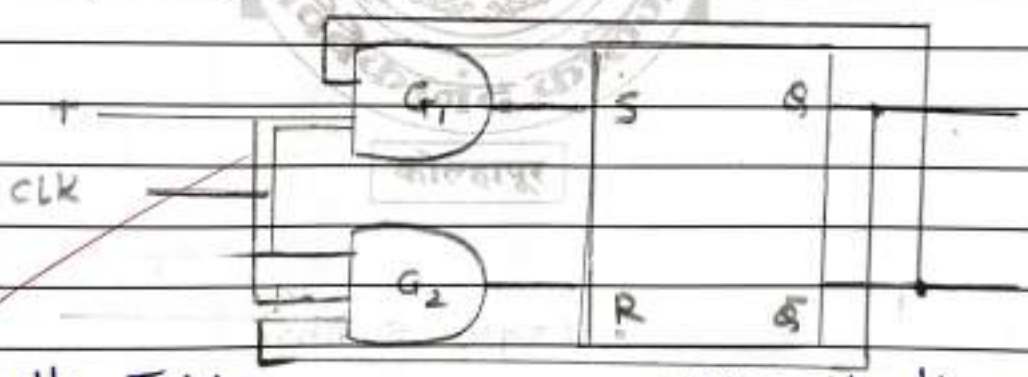
case II : J = 0 , K = 1 When the upper input is low & lower input is high the output goes in reset state.

case III : J = 1 , K = 0 When the upper input is high & lower input is low the output goes in set state.

case IV : J = K = 1 When the both inputs are high then the output goes in toggelling state.

Q 2]

→ T Flip-flop



Truth Table

CLK	T	output
0	x	last state
1	0	0
1	1	1

• circuit diagram.

case I : CLK = 0	case II CLK = 1	case III T = 1
T is don't care condision	T = 0 & the output is low	output is 1

Pradnya Pradip Patil.

।। ज्ञान, विज्ञान आणि सुसंस्कार यांसाठी शिक्षण प्रसार ।।
– शिक्षणमहर्षी डॉ. बापूजी साळुंखे

09086

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Q. 1.

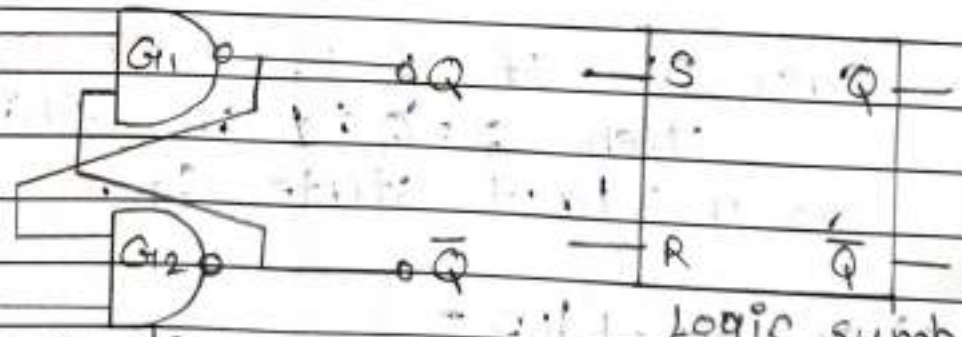
i) a) set

ii) c) Bistable multivibrator

iii) a) Low-to-high transition of clock

Q. 2.

1) R-S latch using NAND gates-



Logic diagram

Logic symbol

When R and S is a input of NAND gate and G_1 and G_2 also. If Q and $\bar{Q}$ are the outputs of NAND gate.

When one of the input is low output is high in NAND gate.

Truth-Table

input		Output action
R	S	
0	0	forbidden
0	1	set (1)
1	0	reset (0)
1	1	last state

Working -

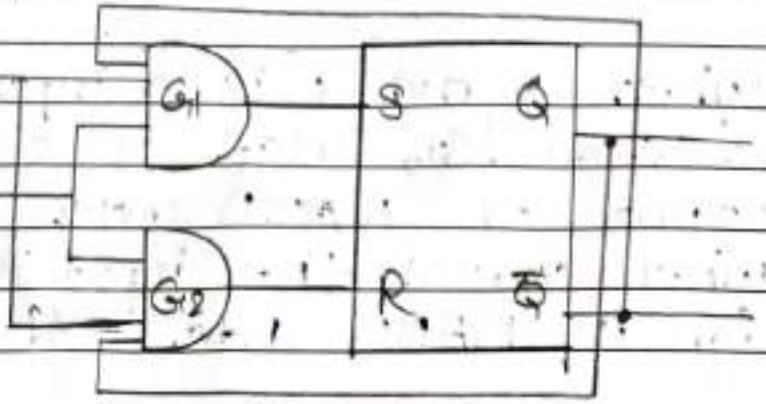
Case -I - If R = 0, S = 0
then the NAND gate of G_1, and G_2 also zero $Q = 0$ but $\bar{Q} = 1$ its state is called as forbidden state.

Case II - If R = 0, S = 1
then G_2 is high and G_1 is low $Q = 1$ but $\bar{Q} = 0$ this state is called setting (set).

Case III - If R = 1, S = 0
then $G_1 = 1$ and $G_2 = 0$ i.e. $Q = 0$, $\bar{Q} = 0$ then state is called as "reset".

Case IV - If R = 1, S = 1
then $Q = \bar{Q} = 1$ i.e. this state is called as a last state Q_n.

9) T flip-flop -



Logic diagram

Input		output
CLK	T	Qn+1
0	X	Last state
1	0	0
↓	1	1

Working -

Case I - If clk = 0 then T is in don't care condition. mean their is no effect on T-flip flope.

Case II - If clk = 1 then

a) T = 0

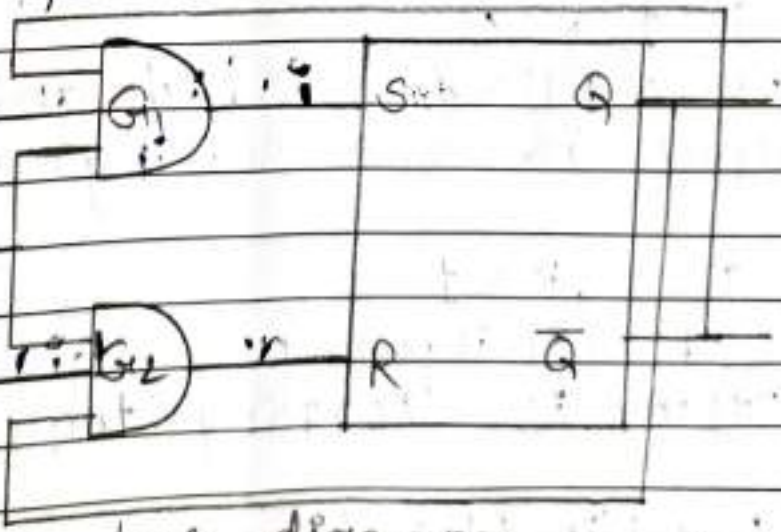
If T is in low state then output is also zero (low).

b) T = 1

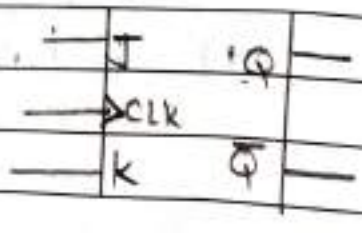
If T is in high state then output is in one (high).

T-flip-flop is also a J-K flip-flop.

4) J-K flip-flop -



Logic diagram



Working -

Case I - If CLK = 0 then the J and K flip-flop is in don't care condition. and output is Qn means last state.

Truth - Table

Input			output
CLK	J	K	
0	x	x	Qn (last state)
1	0	0	Qn (LS)
1	0	1	0 (reset)
1	1	0	1 (set)
1	1	1	Toggling

Case II - If CLK = 1 then

a) J = 0, K = 0

If both inputs are low then output is in last state (Qn). No output of this state.

b) J = 0, K = 1 (low)

If J is in high but K is high then the output state is low reset condition. This reset the state.

c) J = 1, K = 0

If J flip-flop is high and K is low then the output is set (setting) condition.

d) J = 1, K = 1

If both inputs are high (one) then output is Toggling (toggled) condition.

J-K flip-flop is also called T-flip-flop. If behaves like T flip-flop.