Vivekanand College, Kolhapur (Autonomous)
Department of Electronics
Notice

Date: 10.04.2023

All the students of B.Sc. II Electronics are hereby informed that their internal examination for Semester IV will be conducted in offline mode as per attached schedule.

Paper	Section	Section title	Marks	Date	Time
IV DSC - 1005D1	I	Operational Amplifier	15	20.04.2023	04:15 to 05:15 pm
IV DSC- 1005D2	II	Microcontroller 8051	15	21.04.2023	02:30 to 03:30 pm

VIVEKANAND COLLEGE ESTD. JUNE 1964 KOLHAPUR-416 003

(Dr. C. B. Patil)
Head
Department of Electronics
Vivekanand College, Kolhapur.

VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

B.Sc. Part- II (Electronics) (Sem-IV)

Internal Examination 2022 - 23

Course Code: DSE - 1005D

Section - I: Operational Amplifier **Total marks: 15**

20-4-23

Q.1) Select most correct alternatives for the following (one mark each) **[3 Marks]**

1. The main advantage of differential amplifier is that, it rejects ----------
   A) common mode signal B) distortion
   C) differential mode signal D) None of the above
2. An ideal op-amp has ……..input impedance
   A) 75 Ω B) 0 Ω
   C) 2M Ω D) Infinite Ω
3. An integrator op-amp uses --------- element in the feedback path
   A) resistor B) capacitor
   C) inductor D) None of the above

Q.2) Attempt any Three (Four marks each) **[12 Marks]**

1. Explain the common mode rejection ratio (CMRR) and slew rate of op-amp.
2. Compare ideal and practical parameters of op-amp.
3. Explain the working of Op-Amp as voltage follower with circuit diagram.
4. Explain working of op-amp as an adder with neat diagram.
5. Draw circuit diagram of op-amp in inverting amplifier. Find the expression for its output voltage & gain

ज्ञान विज्ञान आणि सुसंस्कार यांसाठी शिक्षणप्रसार"

शिक्षणमहर्षी डॉ. बापूजी साळूंखे

श्री. स्वामी विवेकानंद शिक्षण संस्था, कोल्हापूरचे

विवेकानंद कॉलेज (स्वायत्त),कोल्हापूर.

Internal Examination 2022-23

Class: B.Sc.-II Semester-IV Paper IV DSC-1005D

Date:-21/04/2023 Subject: Microcontroller 8051 Marks: 15

Time 02:30pm to 03:30pm

Q.1 Short answer questions: [Attempt any THREE] [3*5 marks=15 marks]

i. Describe any five logical instructions.
ii. Describe any five arithmetic instructions.
iii. Describe any five Bit manipulation instructions.
iv. Write an assembly language program for 8051 to generate a square wave of 50 KHz with 50% duty cycle on port pin P1.5 using timer 0 in mode 1.
v. Write an assembly language program for 8051 to generate a square wave of 100 KHz with 50% duty cycle on port pin P2.3 using timer 1 in mode 2.

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SUPPLIMENT

Signature of Supervisor: 5/15

Vivek Vasant Buchade

Suppliment No. :

Roll No. : 7724

Class : B.Sc. II

Subject : Electronics I

Test / Tutorial No. : Internal Exam

Div. :

Q.1.

1) The main advantage of differential amplifier is that, it rejects .....

→ (A) Common mode signal.

2) An ideal-op-Amp has ~~input~~ ..... input impendance.

→ (D) Infinite. Ω

3) An Integrator op-amp uses ..... element in the feedback path.

→ (B) Capacitor

3

Q.2.

(1) Common mode refers to the solution where the same voltage is applied to the investing & non-investing inputs.

Common mode rejection has the ability to reject the comm mode single common mode rejection is matimatically defined a

$$CmRR = \left(\frac{AB}{ACM}\right)$$ where,

Ab is the differential gain ACM is the common mode gain Ideal Op-Amp has gain. therefore, the rejection level is satisfied & common mode signal are rejected easily.

(3)

→ If we made the feedback resistor of equal zero & registor f_2 equal to the infinity then the circuit would have fixed gain has '1' has the output voltage would be present on the investine input terminal this woud the produce a Special type of non-inverting amp. called as voltage follower.

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Class : B.Sc. II

Subject : Electronics II

Test / Tutorial No. : Internal Exam

Div. : Microcontroller 8051.

Q.1.

2)

→ Arithmatic Instruction.

1) Addition.

The instruction ADD is used for addition of two operands for addition one of the operand should be present with regester A. the result of addition is always stored in a register flag A. modified to the result.

2) Substraction.

The instruction SUB is used for the substraction of two operands. for substraction one of the operand should be present with register A ~~the result of substraction is always stored in~~ is perform 2's compliment method the result of substraction is always stored in register flag A. modified to the result.

2

3) Increment

The increment is the performed using instructions. INC the operand value is incremented by one flags are not affected upon on execution of these instruction

4) Multiplication —

The 8051 microcontroller has capacity of 8-bit multiplicatio using regestor A & B for multiplication. Register A & B act as source as destination. In 8 bit multiplication of 16 bit result granted, the higher byte is stored in regeste B. & the lower byte is stored in register A. the overflow flag is set its result in the greater than FFH.

5) Dividation.

the 8051 microcontroller has capacity of 8 bit division to control the content of register A. is divided content of regester B. After division quotient is stored in register A & reminder stored in register B. overflow flag is set in result content is divided by zero.

-1)

→ The logical instructions

1)	CLR A	A=0	register specific	CLRA	this instructions circuit content of registor A
2)	CPL A	$\overline{A}$	registor specific	CPLA	the instruction with construction of registor A
3)	RLA	Anticn	registor specific	RLA	the instruction with construct of registor.

4) RRA $An \rightarrow An+1$ | RRA The instruction with the centre + of resistor A of det + by one with throw curry.

SWAPA $A(0-3) \rightleftarrows (A(4-7)$ | SWAPA The instruction with the centre of + resist A to let + by one with through

2+8 = 10/15

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Name :- chavan snehal Bhikaji

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Roll No. : 7925

Class : B.Sc- II (SY)

Signature of Supervisor

Subject : Electronics.

Test / Tutorial No. :

Div. :

Q1

1. The main advantage of differential amplifier is that, it rejects _____

⇒ Common mode signal.

2. An ideal op-amp has ---- input inpedance.

⇒ C] 2MΩ

3] An integrator op-amp uses ---- element in the feedback Path

⇒ B] Capacitor.

Q2.

1. The common mode rejection ratio (CMRR) when the ratio of the op-amp. it is the common mode rejection ratio.
The common mode rejection ratio of the op-amp is inverting and non-inverting of the op-amp.
The Mathematically use of the CMRR

$$CMRR = |A_D / A_{cm}|$$

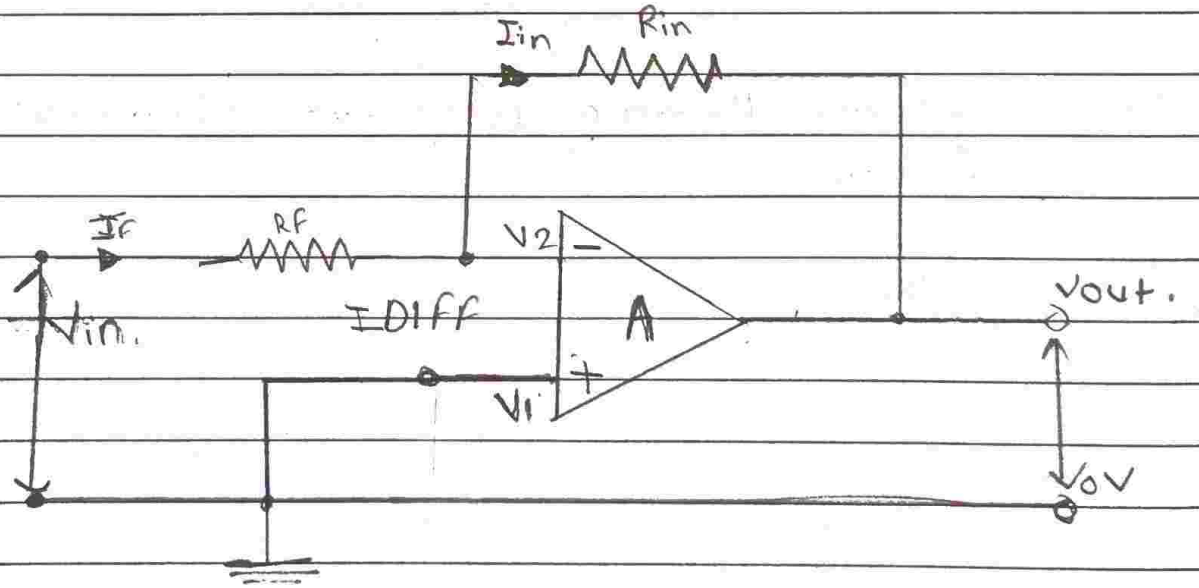
Where A_D is differential ratio of the op-amp. the common mode ratio. The common mode ratio op-amp is the signal.

Acm is very the common mode ratio op-amp..

The common mode rejection ratio is the op amp rejection of the signal op-amp.

Q6

A.



2

Parameters	ideal	Practical
Voltage.	∞	2×10^5
input inpadence z_{in}	∞	$2 M\Omega$
output impedence z_{in}	0	$75\ \Omega$
input offset voltage	0	Infinite Ω
input offset current	0	.
	∞	
CMRR	∞	
	∞	

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Class : B.Sc- II (CSY)

Signature of Supervisor

Subject : Electronics

Test / Tutorial No. : Internal Examination. Microcontroller 8051

Div. :

Q1

i] Logical instruction.

i] Mnemonic — INL A, Rn
operation — A (ANDed) Rn → A
Addressing mode — Register
No-of bytes — 1
Example — INL A R4
Description — The content of register R4 with the ANDed of the register A. The result stored in register A.

ii] ~~INL~~ A, ~~Direct~~
Mnemonic — INL A, Direct
operation — A (ANDed) Rn → A
Addressing mode — Direct
No-of bytes — 2
Example — INL A 20H.
Description — The content of memory location 20 H of the Anded with the content of register A is the result Stored in register A.

iii] Mnemonic — XOR A, Rn
operation — A (XORed) Rn → A
Addressing mode — Register
No. of bytes — 1
Example — XOR A, R4
Destribution
Description — The content of Register R4 with the xored register A. The result in stored is register A.

iv) Mnemonic — XOR A, Direct
operation — A (XORed) Rn →
Addressing mode — Direct
No. of bytes — 2
Example — XOR A, 20 H
Description — The content of the memory location 20 H with XORed register A. The result is stored in register A.

v] Mnemonic — XOR A, Direct.
operation — A (XORed) Rn → A
Addressing mode — Direct
No. of bytes — 2
Example — XOR A, 20H A.
Description — The content in memory location 20 H of the register A. The result in stored is register A.

3 Arithmetic Instruction.

Addition

1] Mnemonic — ADD. Rn

operation — A + Rn → A

Addressing mode — Register

No. of bytes — 1

Example — ADD A, R5

Description — The content in register A5 with added in register A. The result is stored in register A.

Subtraction.

2] Mnemonic — SUBB A. Rn

operation — A − Rn − CY → A

Addressing mode — register

No. of bytes — 1

Example — SUB A. R5

Description — The content in register R5 with the subtracted in register A. The result is stored in register A

4 Increment.

Mnemonic — INC A

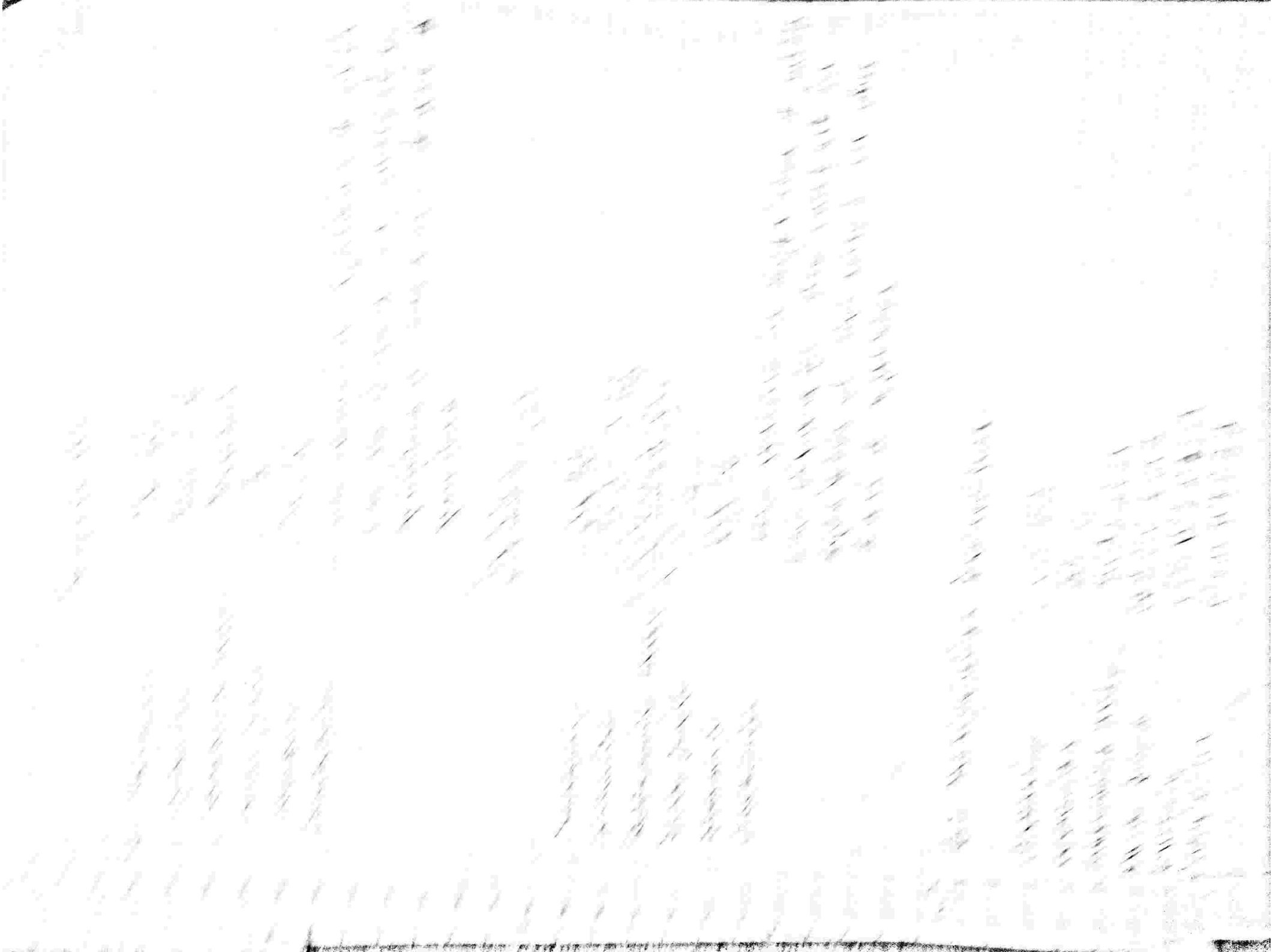
operation — A + Rn → A.

Addressing mode — Register

No. of byte. — 1

Example — INC A. R6

Description — The content of Register R6 is the incremented by one.



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Suppliment No. : 1
Roll No. : 7725
Class : B.Sc- II

Subject :
Test / Tutorial No. :
Div. :

ii] Mnemonic — SETB Bit
operation — Bit = 1
Addressing mode — Reggister
No. of bytes — 1 or 2
Example — SETB P1.0
Description — Set of Bit P1.0

iii] Mnemonic — CLP Bit
operation — Bit = $\overline{Bit}$
Addressing mode — Reggister.
No. of bytes — 1 or 2
Example — CLP 3.1
Description — compliment Bit P3.1

iv] Mnemonic — MOV Bit C.
operation — Bit → CY
Addressing mode — Direct
No. of bytes — 2
Example — MOV C, ACC, 2.
Description — The content of carry bit and the reggister of one 2.

v) Mnemonic — MOV C, Bit
operation — (Cy) → Bit
Addressing mode — Direct
No. of bytes — 2
Example — MOV ACC. C1
Description — The content of carry by register of ~~s~~ two

Sourav Sharad Gadkari

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SUPPLIMENT

Signature of Supervisor	8/15

Suppliment No. :

Roll No. : 7729

Class : B.Sc-II

Subject : Electronics

Test / Tutorial No. : Internal Exam

Div. : A

Section : I

Q1.

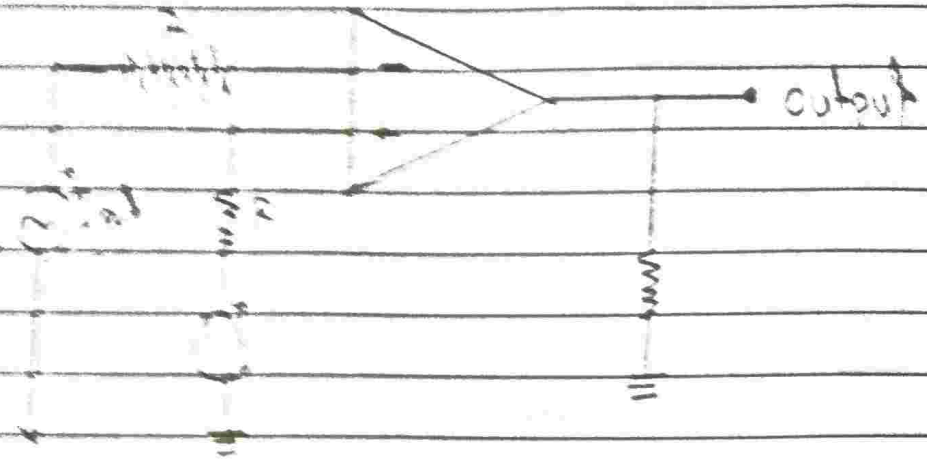
1) The main advantage of differential amplifier is that it rejects ~~common mode signal~~ distortion

ii) An ideal op-amp has Infinite Ω input impedance

3

iii) An integrator op-amp uses capacitor element in the feedback path

iii) Summing Amplifier



iv) Inverting Amplifier

Inverting amplifier is ~~close~~ opposite form non-inverting amplifier and Inverting amplifier is ~~an~~ current flow and terminal Internal output? Inverting amplifier is close loop in inverating ~~amplifier~~ and ~~the~~

Q2) 1. Comman mode Rejecation Ratio (CMRR)

Coomman mode ~~Rejecation~~ refer to the Saitution when thee Same voltage is applied to both the inverting and non-inverting terminal at the op-amp the comman mode rejecation refer of the ability of the op-amp to reject the comman mode Signal The comman mode rejecation ratio refer of the abiliaty of the op-amp to the reject comman mode Signal mathematical defind is

CMRR = Ap / Acul

where Ao is the differnatial gain of the op-amp for idea op amp

As refer to the comman-mode gain of the op amp The CMRR of an ideal op amp is ∞. That mean is is the to reject all comman mode Signal.

3) ex[illegible] on op as voltage follower

4) explain working as adder

5 Draw the

Saurav Bharat Gadkari

7/15

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Signature of Supervisor

Suppliment No. :

Roll No. : 7729

Class : BSc – II

Subject : Electronics (microcontroller 8051)

Test / Tutorial No. : Internal Exam

Div. : A

Q1 iii) Bit manipulation instructions.

	Menmonic	Addersing mode	Example	Desiprotion
i)	CLR Bit	Regesiter direct if oprated on carry bit	CLR P2.3	Clear the bit P2.3
ii)	SETB Bit	Regesiter direct if oprated on carry bit	SETB P1.0	set the bit P1.0
iii)	CPL Bit	Regesiter direct if oprated on carry bit	CPL 3.1	complaiment the bit P3.1
iv)	ANL C, Bit	Direct	ANL C.ACC.3	The idicator perform logically
v)	mov Bit C	Direct	MOV ACC 2C	The carry bit ~~regesite~~ copied regesite bit 1 to carry A

Q1 i) Logically instruction

CLR D	A.0	Regester Amplefeir	CLR D The instruction clear the enters of regicifer
RLA	ANCr = $\overline{A}$	regester 1 CPL Shift	The ~~regesiter~~ instructs of counter of regesiter
RRA	An = An+1	regester 1 RLA Specific	The instruction will Shift the content of resister a left or bit
SWAP	A(n-3) ⇒ An	regester 1 swap Shift	This instruction are change cursur nibble of high nibble of resister

Q1 ii) five. arithematic instrucations

In 8051 microcontroller there are 24 differnation. instrucations under the Arithematic group

In total fure are 64 open code the carry flag (or) Auxilliary carry (AC) and verfication flag (or)

SUB - Substraction

Div - Divied

ADD - Addition

Ananya Netaji Jadhav. 3+8=11/15 ✓

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Suppliment No. :

Roll No. : 7730

Class : BSc - II

Subject : Electronics .

Test / Tutorial No. :

Div. :

Section - I Operational Amplifier.

Q 1]

1]

→ A] Common mode signal

2]

→ D] Infinite Ω.

3]

→ B] capacitor

3

Q.2]

1]

→ Common mode rejection ratio (CMRR) -:

Common mode rejection reference to the when the applied same volume applied to inverting & non-inverting terminal of op-amp. The common mode rejection ratio reference to messure of the ability of the op-amp. reject to the common mode signal. Mathematically it is defined as.

$CMRR = |A_O / A_{CM}|$

where A_O is Diferential gain of the opamp for ∞ is ideal of the OP-Amp.

A_{CM} is the ideal common mode gain of the op-amp. The CMRR is the ided op-amp is ∞.

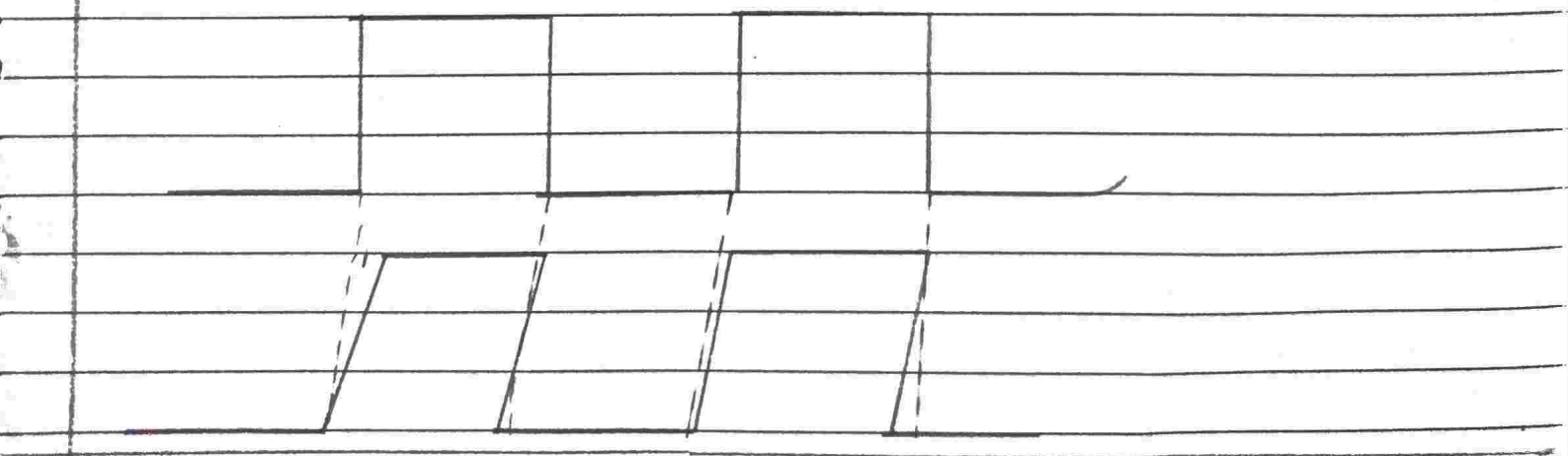
Slew Rate. -:

4 Slew the Rate the m rate of change of output Voltage. with respect to time.

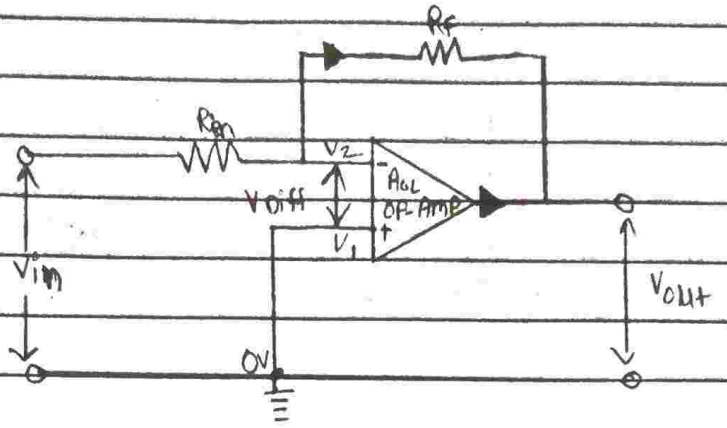
$S_R = dv_o / dt.$

Slew Rate is usually specified V/μs. It is indicate How rapidly output of the op-amp. is change responce to the input.

Slew limited output & input waveform as shown.



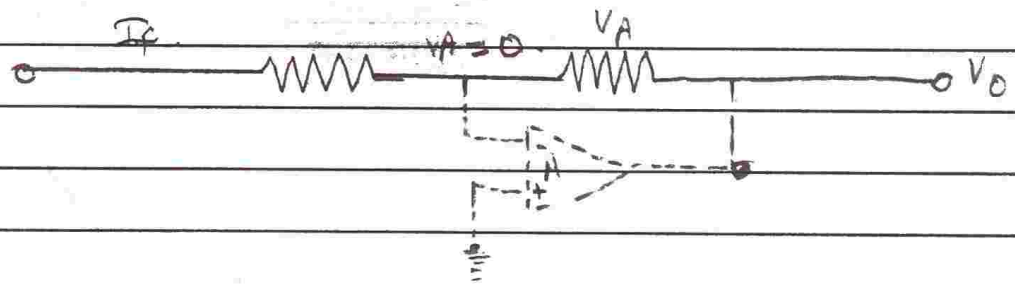
-) 5] Inverting Amplifier.



In this inverting Amplifier circuit the operational amplifier is connected with feedback of Produce when the dealing operational amplifier there are two very important rules remember about inverting amplifier these are.

i] No current flow into Input Voltage and

ii] 'V1 always equal V2'



This because junction is input and feedback signal (x) of some potential of positive (+) input which is Zero Volt and ground then the junction is vertual ground.

$$I_i = \frac{V_i - V_A}{R_i} \quad \text{and} \quad I_f = \frac{V_A - V_o}{R_f}$$

But $V_A = 0$.

$$I_f = \frac{V_i - 0}{R_i} \quad \text{and} \quad I_f = \frac{0 - V_o}{R_f}$$

$$\frac{V_i}{R_i} = -\frac{V_o}{R_f}$$

$$\frac{V_o}{V_i} = -\frac{R_f}{R_i}$$

$$\therefore A_{vf} = -\frac{R_f}{R_i} \quad \text{---------- (1)}$$

$$V_o = \frac{R_f}{R_1} \times V_i \quad \text{---------- (2)}$$

Ananya Netaji Jadhav

13/15

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Suppliment No. :

Roll No. : 7730.

Class : Bsc - II

Subject : Electronics. (Microcontroller 8051)

Test / Tutorial No. : Internal Examination.

Div. :

Q.1] Manipulation instructions –:

Sr. No.	Mnemonic	Operation	Addressing Mode	No of bytes.	Example.	Description
1]	CLR Bit	Bt = 0.	~~op~~ register direct if operated on carry Bit.	1 or 2.	CLR P2.3.	Clear the Bit P2.3.
2]	SETB Bit.	Bt = 1.	register direct if operated on carry Bit	1 or 2.	SETB. P1.0.	SET the Bit P1.0.
3]	CPL. Bit.	Bit = $\overline{Bit}$	register direct if operated on carry Bit	1 or 2.	CPL. 3.1	Compliment the Bit. P3.1
4]	MOV Bit, C.	CY → Bit.	direct	2	MOV ACC.2.	The ~~reg~~ carry register A. copied to Bit number of two.
5]	MOV C, Bit	Bit → CY	direct	2.	MOV C, ACC.1.	The carry Bit number 1 copied to register A.

9] Arithmetic Instruction.

→

	Mnemonic	operation	Addressing mode	NO of Bytes.	Example.	Description.
1]	MUL, AB	A×B → A(0-D) B(0-D)	Register	1	MUL, AB	The content of register A & B. multiplied and store. the result into A and B. register.
2]	SUBB A, Rn	A - Rn (Y → A	Register	1	SUBB A, R1	The content of register Rn and carry Bit subtract. from A register and result store into register A
3]	INC Rn	Rn + 1 → Rn	Register	1.	INC R5	The content of register R5 increment by one.
5]	DEC Rn	Rn - 1 → Rn	Register	1	DEC R5	The content of register R6 Decrment by one.

i] Logical Instruction:-

→

Mnemonic	Operation	Addressing mode.	No. of bytes	Example.	Description.
1] ANL A Rn	A(ANDed) Rn → A.	Register.	1.	ANL A, R4	The content of Registor R 4. ANDed with the content of register A.4.
2] ANL A, [Direct]	A(ANDed) Addr → A	direct	1	ANL A, 20H	The content of memory location 20H ANDed with the content of register 20 H.
3] ANL A, @Rn	A(ANDed). (Rn) → A.	Indirect	1	ANL A, @R5	The content of memory location whose address R5 ANDed with the content of register R5.
4] ANL A # dd+a.	A(ANDed) data → A	Immidiate	2	ANL A, #10H	The immediate dd+a. to ANDed with the content of Register A.
5] ANL Rn, A.	A(ANDed) A → Rn.	Register	2.	ANL R7, A.	The content of Registe A to R7. seleded Registe Bank.

2+8 = 10/15

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VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

SUPPLIMENT

NAME :- Tejupti Arvind Kumbhar

Suppliment No. : 1

Roll No. : 7731

Class : BSc. II nd

Signature of Supervisor	

Subject : Electronics

Test / Tutorial No. : Internal exam.

Div. :

Q1.

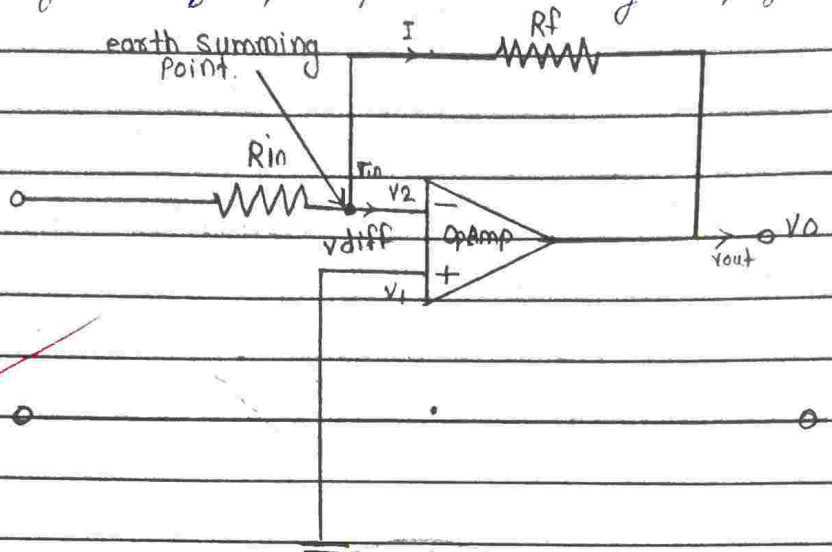
1. The main advantage of differential amplifier is that, it rejects differential mode signal.

2. An ideal op-amp has infinite input impedance.

3. An integrator op-amp uses resistor element in the feedback path.

Q2.

5] Circuit diagram of op-amp in inverting amplifier.



Here given,

$I_i = I_f$

therefore,

$I_i = \frac{V_i - V_A}{R_i}$

and $I_f = \frac{V_A - V_o}{R_f}$

V_A = A = virtual ground therefore $V_A = 0$

$I_i = \frac{V_i - 0}{R_i}$ and $I_f = \frac{0 - V_o}{R_f}$

$I_i = \frac{V_i}{R_i}$ and $I_f = \frac{-V_o}{R_f}$

$$\frac{I_i}{I_f} = -\frac{R_i}{R_f} \quad \text{---------- (1) ..... close loop gain.}$$

$$I_i = -\frac{R_i}{R_f} \times V_i \quad \text{---------- (2)}$$

Q2 1] Common mode rejection ration is known (CMRR).

2] In common mode rejection ratio the voltage is same in the inverting and non-inverting amplifier.

3] Therefore, the equation becomes $\frac{A_D}{A_{CM}}$, where Acm is common mode. ~~and~~

2]

ideal	Practical
Open loop voltage gain	
Input impedence	Infinity
Output impedence	∞

।। ज्ञान, विज्ञान आणि सुसंस्कार यांसाठी शिक्षण प्रसार ।।
– शिक्षणमहर्षी डॉ. बापूजी साळुंखे
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08850

VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

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Subject : electronics.

Test / Tutorial No. : Internal / exam : (microcontroller 8051)

Div. :

1. Logical instructions :-

No.	Mnemonics	operation	Addressing mode	No. of bytes	example	Description
1	CLRA	A = 0	registor specific	1	CLR A	Clear the data / content from the registor A. ie is instruction said
2.	CPL A	$A = \bar{A}$	registor specific	1	CPL A	The insteuction is that the compleme-nt in registor A.
3.	RLA	An+1 = An	registor specific	1	RL A	The content in registor A is shift to the left by one.
4	RRA	An = An+1	registor specific	1	RLA	The content in registor A is shift to the leg by one.
5.	SWAP A	A → A(0.7) A(0.7	registor specific	1	SWAPA	The exchange in higher nibble and lower nibble.

Arithmetic instructions.

Q 2.	No.	Mnemonics	Operation	Addressing Mode	No. of bytes	Example	Description.
INCRE-MENT	1	INC Rn	Rn+1 → Rn	Registor	1	INC R6	The instruction is the content is increase by 1, in registor R6.
DECRE MENT	2.	DEC Rn	Rn-1 → Rn	Registor	1	DEC R6	The instruction is the content is decreases by 1 in registor R6.
MULTI-PLICATION	3.	MUL AB	A×B → A(0.7) B(0.7)	Registor	1	MUL AB	The instruction is the registor A is multiply with registor B and result store in A and B.
DIVI-SION	4	DIV AB	A÷B → A (Quotient) B (Remainder)	Registor	1	DIV AB	The instruction is the registor A and is divide with registor B. and result store in an A & B.
DECI-MAL	5.	DA A.	A → A(BCD)	Registor specific	1	DA A.	The instruction is the registor A is equivalent to B, C & D.

Q3. Bit manupilation instructions.

No.	Mnemonic	operation	Addressing mode	No. of bytes	Example	Description
1.	CLR Bit	Bit = 0	reg. operational on C bit	1/2	CLR P2.3	Clear the content in P2.3
2.	SETB Bit	Bit = 1	reg. operational on CY bit	1/2	SETB, P1.0	set the reg B content in P1.0
3.	CPL Bit	Bit = Bit	reg. operational on CY bit	1/2	CPL P.3.1	Complement to the content P3.1.
4.	MOV Bit, C	CY = Bit	Direct	1/2	MOV C ACC.02	Move the carry to the ACC.0 in reg A of no.2
5.	MOV C, Bit.	Bit = CY	Direct	2	MOV C, ACC.1	Move the carry to ACC.1 in reg A of no.1.