# Vivekanand College, Kolhapur (Autonomous) Department of Electronics

B. Sc-II Semester-III
Internal Examination Feb-2020-21

#### Notice

All the students of B. Sc-II, hereby informed that the internal examination of 20 marks for Feb-2020-21will be conducted as per the below timetable. The examination will be conducted online mode with Google Forms. Attend the examination on your place on time given in time table. The nature question paper is multiple-choice questions. The syllabus for internal examination will be syllabus covered still 6<sup>th</sup> feb.2021.

#### Time table

			10.4	Time
Sr.	Code and Name of paper	Section	Day and Date	Time
No	DSE 1005C :		Tuesday,	
1	Electronics Communication and Microprocessor 8085	I &II	9 <sup>th</sup> feb,2021	11.30 am-12.30

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Head of Department Head

Department of Electronics Vivekanand College, Kolhayur.



## Vivekanand College, Kolhapur (Autonomous) B.Sc-II (Sem-III) Internal Exam-2021\_ Electronics

Paper No-III

Section-I& II

Subject Code: DSC-1005C

Name of Paper: Electronics Communication and Microprocessor 8085

Data: 09 /02/2021

Time:11.30 am to 12.30 pm

Total Marks: 20 Instructions:

- 1.All Questions are compulsory.
- 2.Each Question carries 1 Marks.
- 3. Figure to write indicate full marks.
- \* Indicates required question
- 1. Email \*
- Student name (First name\_Middle name\_Last name) \* 2.
- 1. ----- is the name given to simultaneous two-way communication.

Mark only one oval.

Simplex

half duplex

Full duplex

None of these



19. 17. has the highest interrupt priority.

Mark only one oval.

RST 7.5

RST 6.5

RST 5.5

TRAP

20. 18. ---- register is used to indicate the status of the result.

Mark only one oval.

ACC

) B

Flag

PC

21. 19. Zero flag =1, which means the result is ------

Mark only one oval.

Non zero

Zero

1

None of these

22. 20. Parity flag = 1, indicates the result has ---- parity

Mark only one oval.

Even

Odd

Not defined

None of these



# Vivekanand College, Kolhapur (Autonomous) Department of Electronics B. Sc. II Sem IV Internal Examination Feb 2020-21 Notice

Date: 19.07.2021

All the student of B.Sc.-III hereby informed that, the internal exam of Electronics Sem IV will be held in **online mode with Google forms**. The detail time table is given below.

Paper	Section	Section title	Marks	Date	Time
IV DSC - 1005D	I & II	Advanced Communication & Microcontroller 8051	20	23.07.2021	11:00 am to 12:00pm



(Mr. D. M. Panhalkar)

Head
Department of Electronics
Vivekanand College, Kolhapur.

Paper No-IV

Subject Code: DSC-1005D

### Vivekanand College, Kolhapur (Autonomous) B.Sc-II (Sem-IV) Internal Exam-July-2021 Electronics

Section-I& II

	ivalle of Paper: Advar	nce Communication and Microcontroller 8051
	Data: 23 /07/2021	Time:11.00 am to 12.00 am
	Total Marks: 20	
	Instructions:	
	1.All Questions are co	mpulsory.
	2. Each Question carrie	
	3. Figure to write indica	ate full marks.
*!	ndicates required ques	tion
1.	Email *	
2.	Student name (Fi	rst name_ Middle name_Last name) *
3.	Amplitude of pulsisignal is called	se train varies according to instantaneous value of modulating
	Mark only one oval.	
	PWM	
	PAM	
	PCM	
	PDM	



20.	18. The total number of register banks in 8051 microcontroller are
	Mark only one oval.
	□1
	2
	3
	4
21.	19. A logic on RST pin resets the 8051 microcontroller.
	Mark only one oval.
	Low
	High
	high impedance
	none of these
22.	20. In 8051 RAM space, bit addressable area starts from
	Mark only one oval.
	10H to 1FH
	20H to 2FH
	30H to 3FH
	40H to 4FH

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# Vivekanand College, Kolhapur (Autonomous) Department of Electronics B. Sc-III Semester-V

Internal Examination Feb-2020-21

#### Notice

All the students of B. Sc-III, hereby informed that the internal examination of 20 marks for Feb-2020-21 will be conducted as per the below timetable. The examination will be conducted online mode with Google Forms. Attend the examination on your place on time given in time table. The nature question paper is multiple-choice questions.

#### Time table

Sr. No	Code and Name of paper	Section	Day and Date	Time
1	DSE 1005E1: Linear Integrated Circuits, 8051 Microcontroller Interfacing and Embedded C	I &II	Monday, 8 <sup>th</sup> feb,2021	11.30 am-12.30
2	DSE 1005E1 : Instrumentation, Antenna and Wave Propagation	I &II	Wednesday, 10 <sup>th</sup> feb,2021	11.30 am-12.30

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Head of Department
Head
Department of Electronics
Vivekanand College, Kolhapur



### Vivekanand College, Kolhapur (Autonomous)

Internal Examination (2020-2023)
Class:-B.Sc-III
Paper:-Linear Integrated Circuits

Sem:-V Marks:-10 Subject:-Electronics date:-10/01/2022

* Ind	icates required question		
" HIV	icores and an area of the control of		
1.	Email *		
2.	Roll Number *		
3.	Name of the student *		
4.	Mobile Number *		
5	. 1. The main advantage of differenti	al amplifier is that it rejects *	
	Mark only one oval.		
	Common mode signal distortion		23
	differential mode signal noise		
	Hoise		



1	Z. Oliset Hull pills provided	∪ I ∪ /4 I ale
F	Mark only one oval.	
	2 and 4	
	3 and 5	
	1 and 5	
	none of these	
Q.2	? : Attempt any two	
7.	1. Explain any four paran op-amp amplifier circuit the neat circuit diagram.  5.1.	seters of OP-amp 2. Explain block diagram of * 3.Explain basic differential amplifier using basic differential 4. Explain current mirror circuit with
	Files submitted:	

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	Z. Oliset Hull pills provided to	IU /41 ale		
1	Mark only one oval.			
	2 and 4			
	3 and 5			
	1 and 5			
	none of these			
Q.	2 : Attempt any two			
7.	Explain any four parameter op-amp     3. amplifier circuit	Explain basic differen	2. itial amplifi	Explain block diagram of * er using basic differential
	the neat circuit diagram.	4.	Explain (	current mirror circuit with

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Files submitted:



Paper No-VI

Subject Code: DSC-1005E2

## Vivekanand College, Kolhapur (Autonomous) B.Sc-III (Sem-V) Internal Exam-2021\_ Electronics

Section-I & II

D	Pame of Paper: Instrumentation, Antenna and Wave Propagation Pata: 10/02/2021 Time:11.30 pm to 12.30 pm Potal Marks: 20
	nstructions:
	.All Questions are compulsory.
	Each Question carries 1 Marks.
3	Figure to write indicate full marks.
* In	dicates required question
1.	Email *
2.	Name of the Student (First Name _Middle Name_Last Name) *
3.	1. The radiation pattern is a dimensional quantity.
	Mark only one oval.
	One
	Two
	Three
	None of the mentioned



17.	15. Which of the following thermocouple material combination provides a higher voltage and higher temperature range?
	Mark only one oval.
	chromel-alumel
	chromel-constantan
	copper-constantan
	iron- constantant
18.	16. The main sensing element used in the piezoelectric transducer is
	Mark only one oval.
	thermocouple
	quartz crystal
	LDR
	None of these
19.	17. Strain gauge is a type transducer
	Mark only one oval.
	temperature
	Pressure
	Optical
	None of these
20.	18. LVDT is a type of transducer
	Mark only one oval.
	temperature
	Active Land CO
	Passive ESTD. JUNE
	None of these

#### B. Sc. III Sem VI Internal Examination Feb 2020-21 Notice

Date: 14/06/2021

All the student of B.Sc.-III hereby informed that, the internal exam of Electronics Sem VI will be held in **online mode with Google forms**. The detail time table is given below.

Paper	Section	Section title	Marks	Date	Time
DSE 1005F1	I & II	Industrial Process control, PLC Programming and Advanced Microcontroller	20	23/06/2021	01.15pm to 02.15 pm
DSE 1005F2	I & II	Power Electronics, FPGA & VHDL Programming	20	21/06/2021	11.30 am to 12.30 pm

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(Mr. D. M. Panhalkar)

Head
Department of Electronics
Vivekanand College, Kolhapur.

# B.Sc. Electronics part-III Semester-VI Internal Examination 2021

Subject: Electronics

Name of Paper: Advanced Microcontroller and Embedded System

Date:23/06/2021 Time: 1.15pm to 2.15pm

Total Marks: 10

\* Indicates required question

1.	Email *

2.	Full	Name	of	Student:	*

3.	Seat	Number:	7

4.	Embedded system	is combination of	
----	-----------------	-------------------	--

Mark only one oval.

hardware and software

hardware

software

none of these



Subject Code: DSC-1005F2

Paper No-VI

# Power Electronics-Internal Exam-Sem VI-2021

Section-I & II

N	ame of Paper: Power	Electronics			
	ata: 21/06/2021		pm to 12.30 p	m	
To	otal Marks: 20				
In	structions:				
	.All Questions are con				
	Each Question carrie	and the state of t			
3.	Figure to write indica	te full marks.			
Inc	dicates required quest	ion			
١.	Email *				
2.	Name of the stude	ent (First Name	Middle Nan	ne Last Nam	ie) *
3.	Roll number *				
4.	1) A p-n junction d	iode is a	switchi	ng device .	
	Mark only one ova	l.			
	Unidirectiona	i			
	Bi-directional				
	Multidirection	nal			
	none of the a	hove	110		
	none of the a	5575	HANAND	150	
			S STE		
			1964	4 (5)	

# Vivekanand College Kolhapur(Autonomous) Internal Exam B.Sc-III ,Sem-VI (2020-2021) FPGA and VHDL

### Programming B.Sc-III

* ir	dicates required question			
1.	Email *			
2.	Roll No: *			
3.	Name of the student *			
4.	1. The FPGA refers to  Mark only one oval.	_*		2 point
	First programmable Gate Array Field Programmable Gate Array First Program Gate Array Field Program Gate Array			



0.	<ol><li>The complex programmable logic device (CPLD) contains several F and</li></ol>	PLD blocks * 2 points
	Mark only one oval.	
	a language compiler	
	AND/OR Array	
	a global interconnection network	
	field programmable switches	
6.	3. Programmable Array Logic (PAL) *	2 points
	Mark only one oval.	
	Programmable AND array and programmable OR array	
	Programmable AND array and fixed OR array	
	Fixed AND array and fixed OR array	
	None of these	
7.	4. The full form of VLSI is*	2 points
	Mark only one oval.	
	Very Long Single Integration	
	Very Least Scale Integration	
	Very Large Scale Integration	
	Very Long Scale Integration	
8	5. Families of FPGA is/are *	2 points
	Mark only one oval.	
	Xilinx	
	Altera	
	Actel	
	All of these	



6. Programmable Read Only Men	nory is *	2 points
Mark only one oval.		
One time programmable		
two time programmable		
Many time programmable		
none of these		
10. 7. Which is not part of FPG	A? *	2 points
Mark only one oval.		
Configurable logic block.		
Interconnects		
Switch blocks		
micro-processor		
11. 8. An Antifuse programming	technology is associated with*	2 points
Mark only one oval.		
CPLDs		
SPLDs		
FPGAs		
ASICs		
12. 9. PLAs, CPLDs, and FR	PGAs are all which type of device? *	2 points
Mark only one oval.		
SRAM		
EPROM		
PLD		
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Mark only one oval.

A channel

A line

A flip-flop

A strobe

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