Vivekanand College, Kolhapur (Autonomous)
Department of Electronics
Internal Examination Notice
(B.Sc-III)

Date: 15/07/2021

Course/Subject Name: DSE 1005F2 Section-II FPGA&VHDL Programming

All the students hereby informed that, there will be an online test of 20 marks. The test will be conducted through the Google Platform on 22/07/2021 (Thursday).The Google form link will be sent on what's app group 5 min before commencement of the exam.

Date: 22/07/2021

Time: 11.00 am

Platform: Google form

Test Duration: 1Hr

Dr. P. S. Jadhav
Subject Teacher

Head of the Department

HEAD
DEPARTMENT OF ELECTRONICS
VIVEKANAND COLLEGE, KOLHAPUR
(AUTONOMOUS)

VIVEKANAND COLLEGE ESTD. JUNE 1964 KOLHAPUR-416 003

Vivekanand College Kolhapur(Autonomous) Internal Exam B.Sc-III ,Sem-VI (2020-2021)
FPGA and VHDL Programming

Marks : 20 Subject code: DSE1005F2 Section -II Date: 22/07/2021

* Indicates required question

1. Email *

2. Roll No: *

3. Name of the student *

4. 1. The FPGA refers to _____ * 2 points

Mark only one oval.

- First programmable Gate Array
- Field Programmable Gate Array
- First Program Gate Array
- Field Program Gate Array

5. 2. The complex programmable logic device (CPLD) contains several PLD blocks and..... * 2 points

Mark only one oval.

- a language compiler
- AND/OR Array
- a global interconnection network
- field programmable switches

6. 3. Programmable Array Logic (PAL)..... * 2 points

Mark only one oval.

- Programmable AND array and programmable OR array
- Programmable AND array and fixed OR array
- Fixed AND array and fixed OR array
- None of these

7. 4. The full form of VLSI is _____ *

2 points

Mark only one oval.

- Very Long Single Integration
- Very Least Scale Integration
- Very Large Scale Integration
- Very Long Scale Integration

8. 5. Families of FPGA is/are..... *

2 points

Mark only one oval.

- Xilinx
- Altera
- Actel
- All of these

9. 6. Programmable Read Only Memory is..... *

2 points

Mark only one oval.

- One time programmable
- two time programmable
- Many time programmable
- none of these

10. 7. Which is not part of FPGA? *

2 points

Mark only one oval.

- Configurable logic block.
- Interconnects
- Switch blocks
- micro-processor

11. 8. An Antifuse programming technology is associated with _____ *

2 points

Mark only one oval.

- CPLDs
- SPLDs
- FPGAs
- ASICs

2. 9. PLAs, CPLDs, and FPGAs are all which type of device? * 2 points

Mark only one oval.

- SRAM
- EPROM
- PLD
- SLD

13. 10. Vertical and horizontal directions in FPGA are separated by_____ * 2 points

Mark only one oval.

- A channel
- A line
- A flip-flop
- A strobe

Internal Examination .BSc-III Subject:FPGA & VHDL Programming

Sr	Timestamp	Email Address	Roll No:	Name of the student	Score
1	7/22/2021 11:24	gauribedakar2601@gmail.com	8189	Gauri Rahul bedagkar.	18 / 20
2	7/22/2021 11:24	durga.yadav28092000@gmail.com	8205	Durga vaijanath yadav	18 / 20
3	7/22/2021 11:35	shrutikagujar786@gmail.com	8195	Shrutika sudhir gujar	18 / 20
4	7/22/2021 11:35	snehalchougule2018@gmail.com	8191	Snehal mohan chougule	18 / 20
5	7/22/2021 11:36	maddymane12@gmail.com	8198	Malhar Mane	20 / 20
6	7/22/2021 11:37	karangharale3908@gmail.com	8193	Karan M Gharale	20 / 20
7	7/22/2021 11:39	vilasdandgule1998@gmail.com	8192	Vilas Dandgule	20 / 20
8	7/22/2021 11:39	com	8196	RAJENDRA	20 / 20
9	7/22/2021 11:39	tc991818@gmail.com	8190	Tushar chougale	16 / 20
#	7/22/2021 11:43	dipaksutar1999@gmail.com	8204	Dipak Vishwanath Sutar	20 / 20
#	7/22/2021 11:43	kambleashish2545@gmai.com	8197	Ashish Sunil Kamble	18 / 20
#	7/22/2021 11:45	siddhesh4249@gmail.com	8203	Siddhesh shivaji shinde	20 / 20
#	7/22/2021 11:45	ksarnaik78@gmail.com	8200	Kunal ketan sarnaik	20 / 20
#	7/22/2021 11:47	shreyaspowar26@gmail.com	8199	Shreyas Sunil Powar	20 / 20
#	7/22/2021 11:49	ghorpade.sunil2000@gmail.com	8194	Sunil Uttam Ghorpade	20 / 20
#	7/22/2021 11:51	siddharthashete@gmail.com	8201	Siddharth shete	18 / 20

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