Semester- III Paper- III

DSC -1005 C: Electronics Communication and Microprocessor 8085

Section II: Microprocessor 8085

UNIT 2: 8085 Microprocessor Architecture

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8085 Microprocessor Architecture:

Architecture of 8085 Microprocessor:

Salient features of 8085, Block diagram and Pin description of 8085, Data and address bus, Registers, ALU, Stack pointer, Program counter, Flag register, Clock and reset circuits. Interrupts in 8085, Demultiplexing of AD0-AD7.T-states, Machine cycle, Instruction cycle, Timing diagram of MOV and MVI instrucitons.

1. 8085μp was manufactured by INTEL.

2. It is 40 pin IC manufactured using N-MOS technology.

3. It is an 8-bit microprocessor i.e. it can accept, process or provide 8-bit data simultaneously.

4. It operates on a single +5V power supply connected at Vcc

5. It operates on clock cycle with 50% duty cycle.

6. It has on chip clock generator. This internal clock generator requires tuned circuit like LC, RC or crystal. The internal clock generator divides oscillation frequency by 2 and generates clock signal, which can be used for synchronizing external devices.

7. It can operate with 3 MHz clock frequency.

8. It has 16 address buses, hence it can access 2^{16} =64 Kbytes of memory.

9. It provides 8 bit I/O address to access (2^8) =256 I/O ports.

10. In 8085, the lower 8-bit address bus (A_0-A_7) and data bus (D_0-D_7) are multiplexed to reduce number of external pins. But due to this, external hardware is required to separate address lines and data lines.

11. It supports 74 instructions with following addressing modes. (a) Immediate, (b) Register, (c) Direct (d) Indirect (e) Implied.

12. The Arithmetic logic unit of 8085 performs a) 8 bit binary addition with or without carry. (b) 16 bit binary addition (c) 2 digit BCD addition (d) 8-bit binary subtraction with or without borrow (e) 8-bit logical AND, OR, EX-OR, complement (NOT) and bit shift operations.

13. It has 8-bit accumulator, flag register, instruction, register, six 8-bit general purpose. Registers (B, C, D, E, H and C) and five 16-bit registers (SP and PC)

14. It provides five hardware interrupts: TRAP, RST 7.5. RST 6.5, RST 5.5 and INTR.

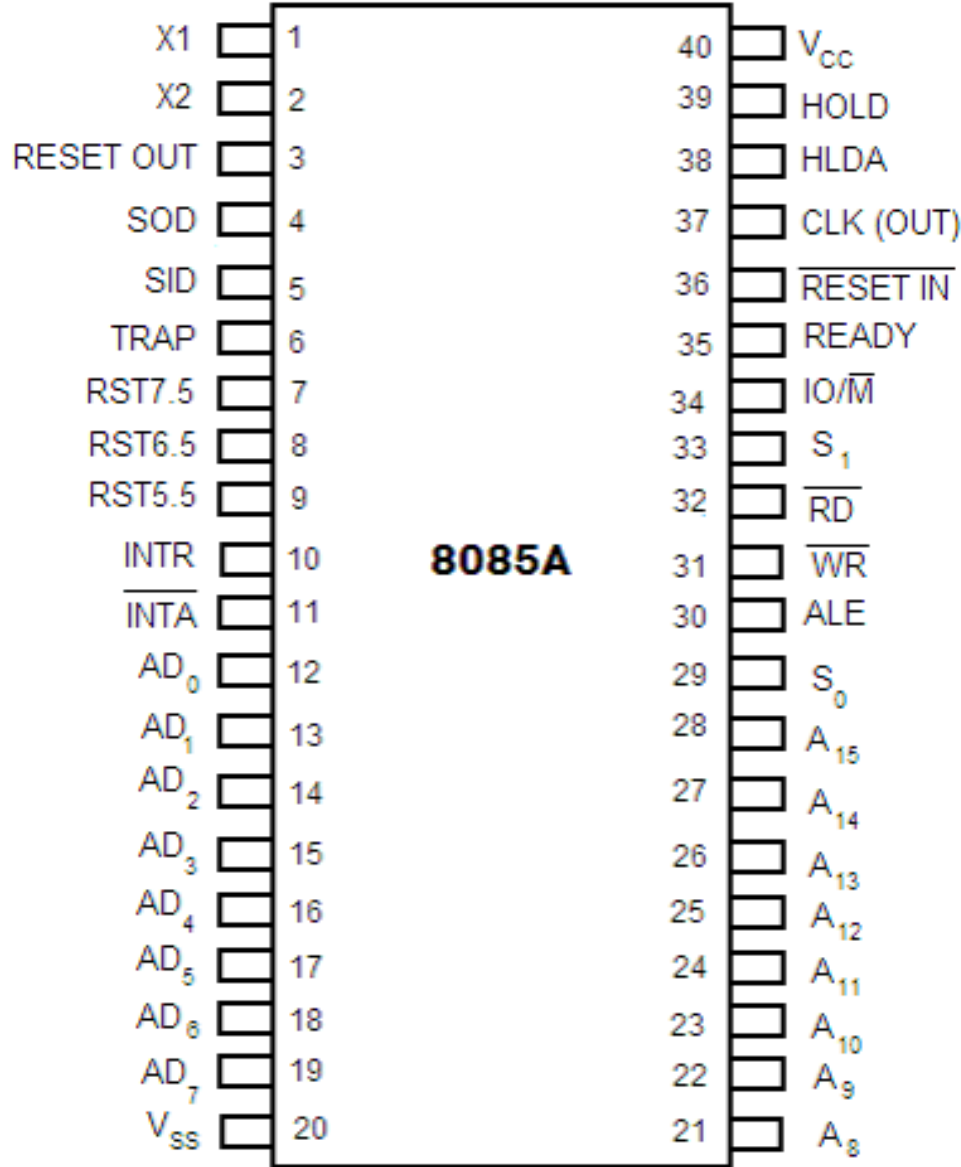15. It has serial I/O control which allows serial communication.

16. It provides control signals (RD, WR) to control bus cycles.

17. The status signals (IO /M, S0, S1) decides which type of machine cycle microprocessor is executing.
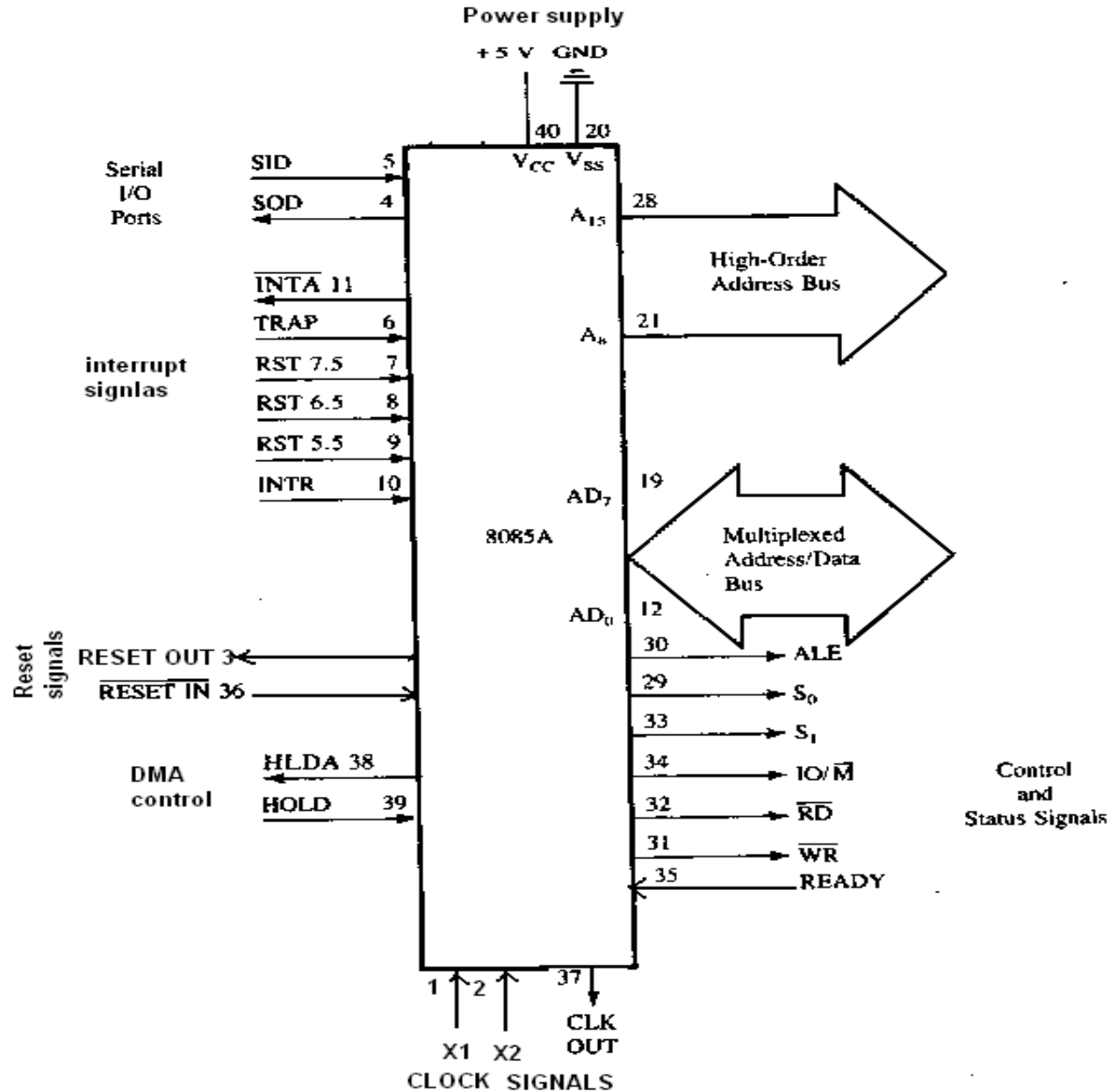
18. It has mechanism by which it is possible to increase its interrupt handling capacity.

19. The 8085 has an ability to share system bus with direct memory access controller. This feature allows to transfer large amount of data from I/O device to memory or from memory to I/O device with high speeds.
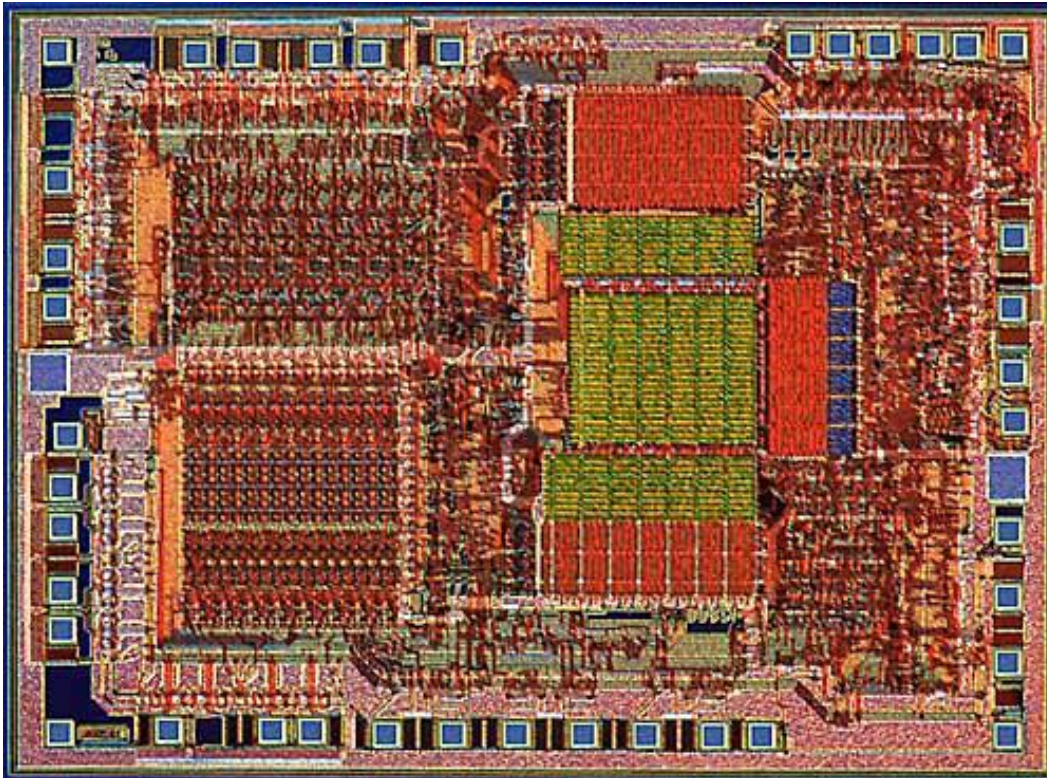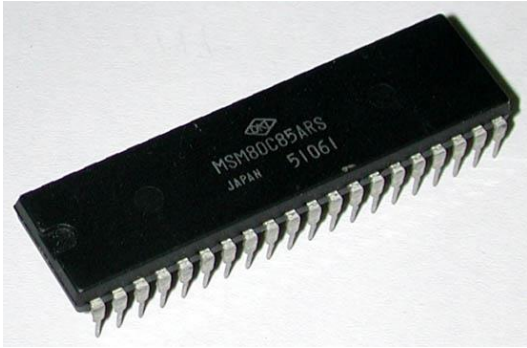
Pin diagram of 8085

|		
X1	1	40	Vcc
X2	2	39	HOLD
RESET OUT	3	38	HLDA
SOD	4	37	CLK (OUT)
SID	5	36	$\overline{\text{RESET IN}}$
TRAP	6	35	READY
RST7.5	7	34	IO/$\overline{\text{M}}$
RST6.5	8	33	S_1
RST5.5	9	32	$\overline{\text{RD}}$
INTR	10	31	$\overline{\text{WR}}$
$\overline{\text{INTA}}$	11	30	ALE
AD_0	12	29	S_0
AD_1	13	28	A_{15}
AD_2	14	27	A_{14}
AD_3	15	26	A_{13}
AD_4	16	25	A_{12}
AD_5	17	24	A_{11}
AD_6	18	23	A_{10}
AD_7	19	22	A_9
V_{ss}	20	21	A_8

8085A

8085 signal diagram

Intel 8085 Microprocessor

- Introduced in 1974
- 8-bit architecture
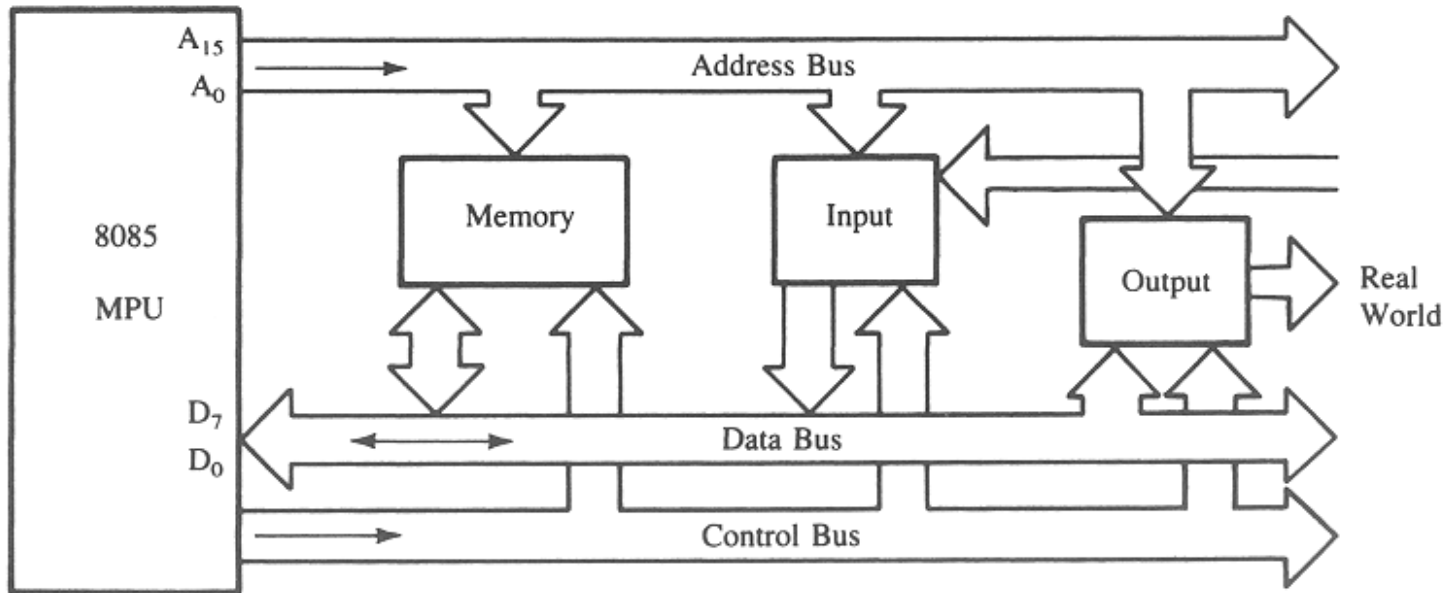- Still used in some microcontroller applications !

8085 Functional Block Diagram
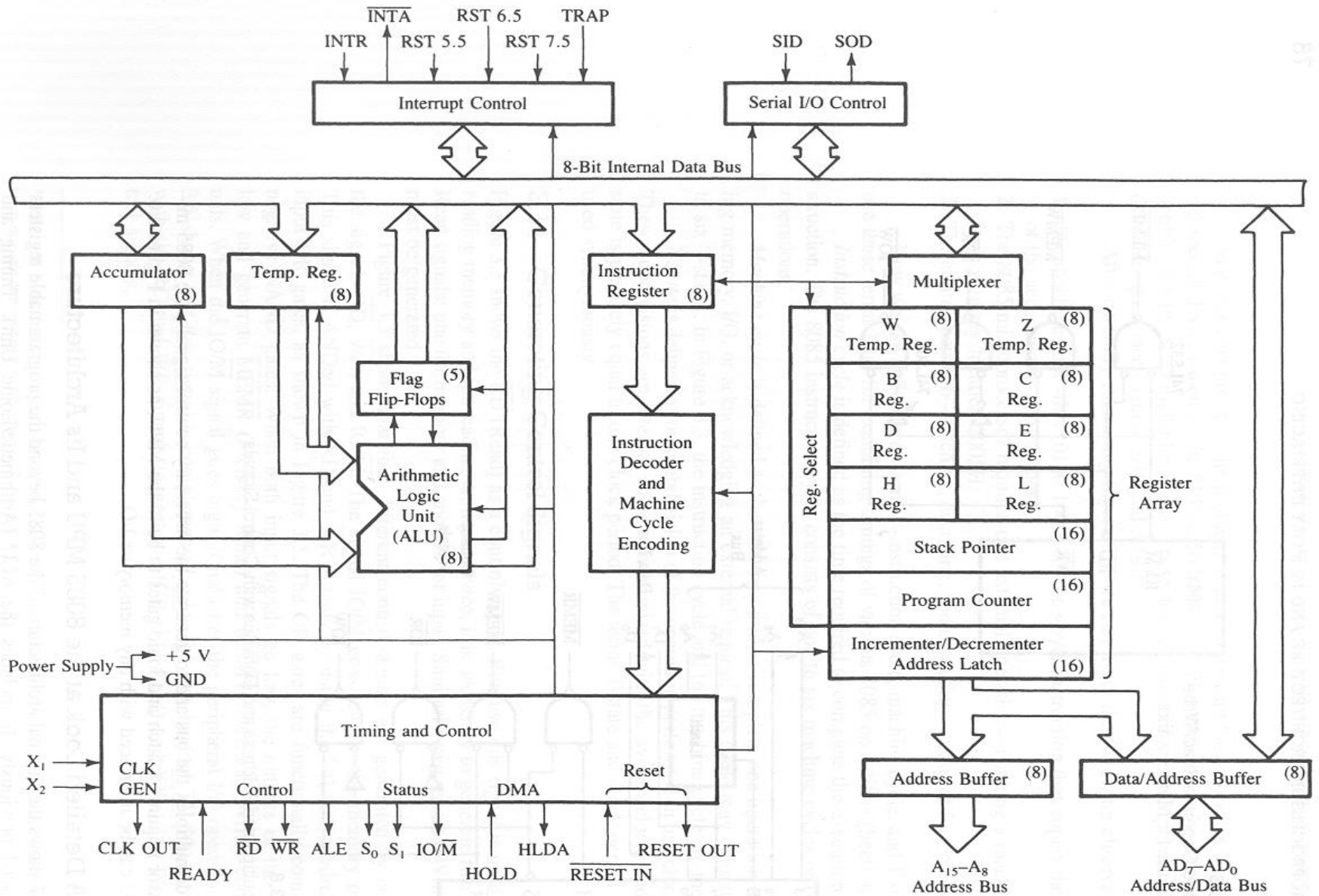
The 8085 Bus Structure

The 8-bit 8085 CPU (or MPU – Micro Processing Unit) communicates with the other units using a 16-bit address bus, an 8-bit data bus and a control bus.

The 8085 Bus Structure

Address Bus

- Consists of 16 address lines: $A_0 - A_{15}$

- Operates in **unidirectional** mode: The address bits are always sent from the MPU to peripheral devices, not reverse.

- 16 address lines are capable of addressing a total of $2^{16} = 65,536$ (64k) memory locations.

- Address locations: 0000 (hex) – FFFF (hex)

The 8085 Bus Structure

Data Bus

- Consists of 8 data lines: $D_0 - D_7$

- Operates in **bidirectional** mode: The data bits are sent from the MPU to peripheral devices, as well as from the peripheral devices to the MPU.

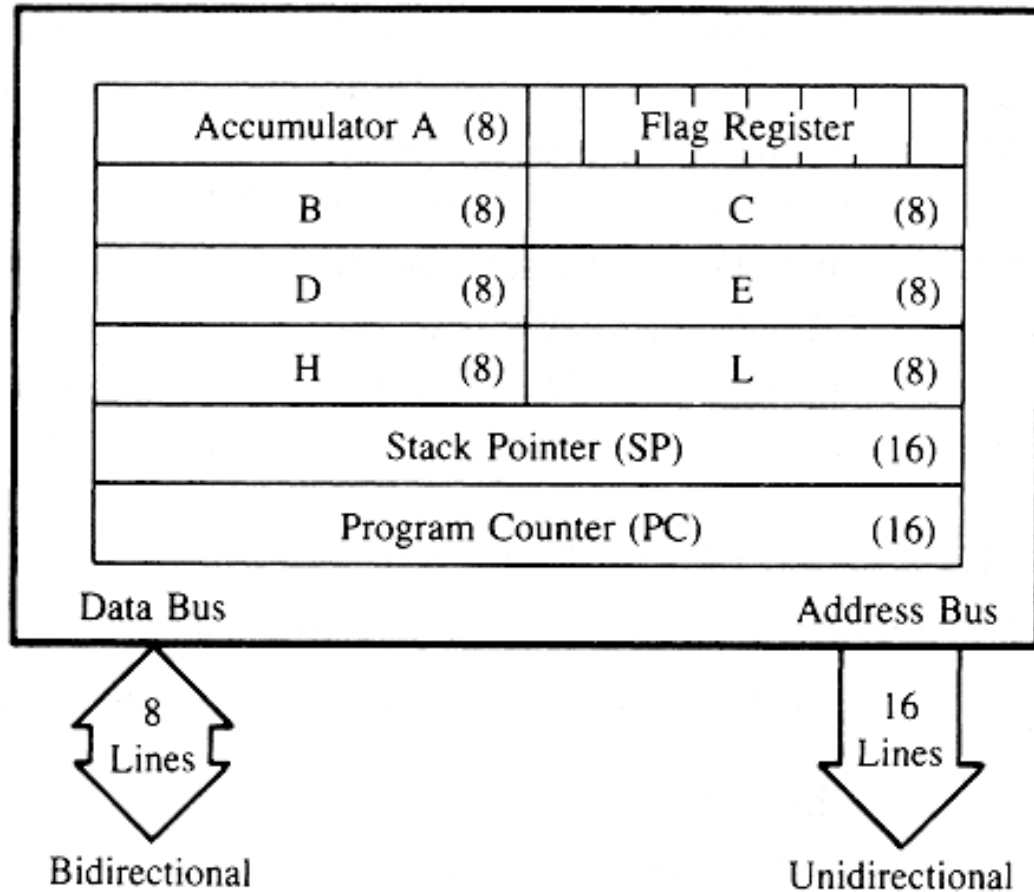- Data range: 00 (hex) – FF (hex)

Control Bus

- Consists of various lines carrying the control signals such as read / write, enable etc.

The 8085: CPU Internal Structure

The internal architecture of the 8085 CPU is capable of performing the following operations:

- Store 8-bit data (Registers, Accumulator)

- Perform arithmetic and logic operations (ALU)

- Test for conditions (IF / THEN)

- Sequence the execution of instructions

- Store temporary data in RAM during execution

The 8085: Registers

Accumulator A (8)		Flag Register	
B	(8)	C	(8)
D	(8)	E	(8)
H	(8)	L	(8)
Stack Pointer (SP)			(16)
Program Counter (PC)			(16)

Data Bus — Address Bus

8 Lines — Bidirectional

16 Lines — Unidirectional

The 8085: CPU Internal Structure

Registers

- Six general purpose 8-bit registers: B, C, D, E, H, L

- They can also be combined as register pairs to perform 16-bit operations: BC, DE, HL

- Registers are programmable (data load, move, etc.)

Accumulator

- Single 8-bit register that is part of the ALU !

- Used for arithmetic / logic operations – the result is always stored in the accumulator.

Flag register
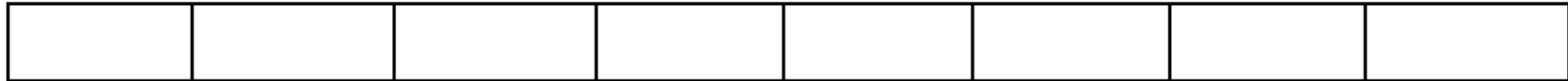
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	**Z**		**AC**		**P**		**CY**

Flag Bits

- Indicate the result of condition tests.

- Sign , Zero, Auxiliary Carry, Parity and Carry

- Conditional operations (IF / THEN) are executed based on the condition of these flag bits.

1. sign flag[S]- indicates the sign of a value(result) calculated by an arithmetic or logical instruction. S=0 , Result=+ve & S= 1, Result= -ve

2. zero flag[Z]- is set to 1 if an arithmetic or logical operation produces a result of 0; otherwise set to 0.

3. parity flag[P]- is set to 1 if the result of an arithmetic or logical operation has an even number of 1's; otherwise it is set to 0.

4. carry flag [CY]- is set when an arithmetic operation generates a carry out.

5. auxiliary carry flag [AC]- very similar to CY, but it denotes a carry from the lower half of the result to the upper half.

The 8085: CPU Internal Structure

Program Counter (PC)

- Contains the memory address (16 bits) of the instruction that will be executed in the next step.

Stack Pointer (SP)

- a sixteen bit register used as a stack memory pointer. PUSH and POP instructions are used to access stack memory.
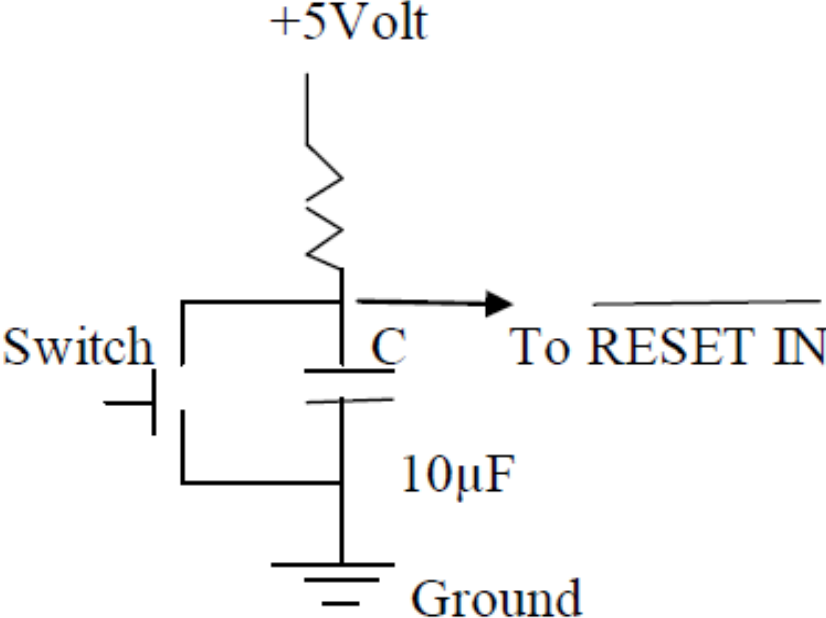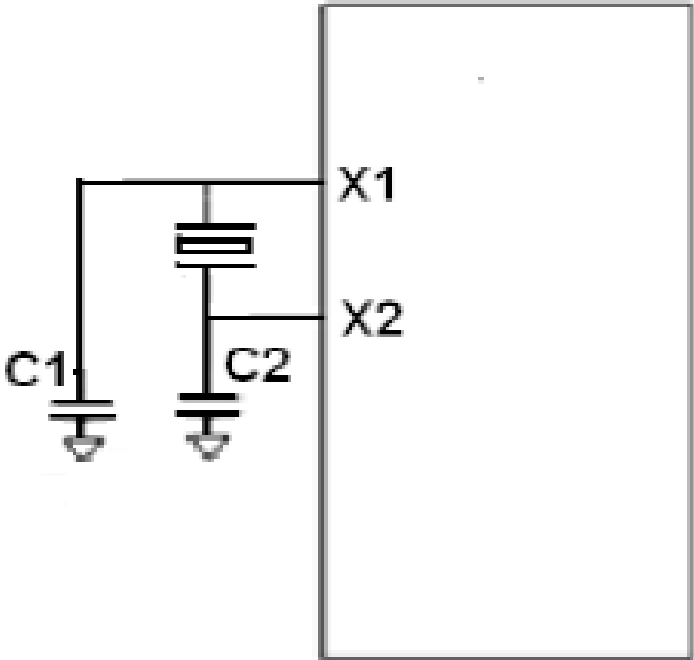
Internal structure of ALU
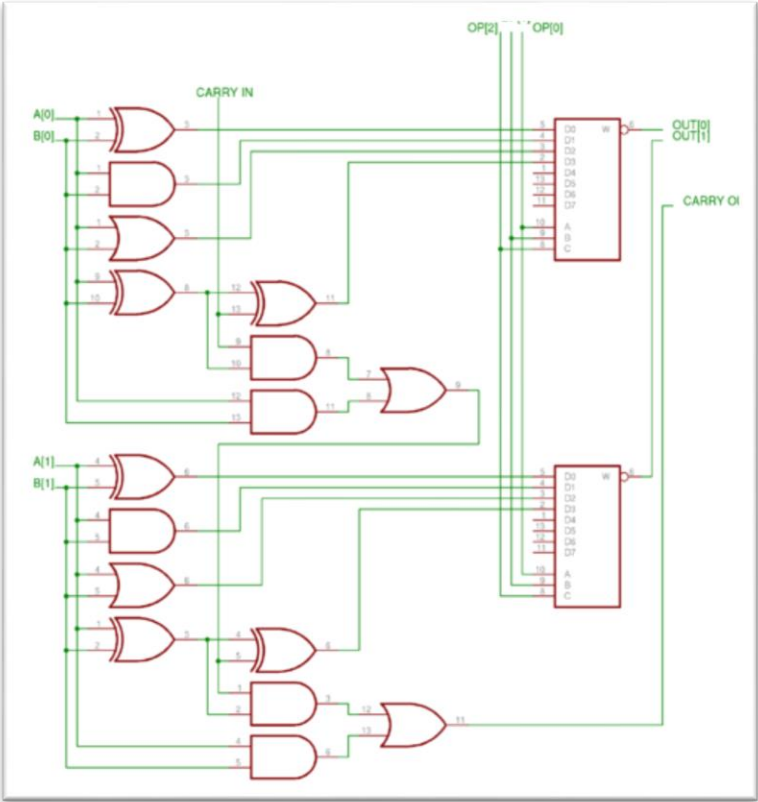

2 bits of ALU
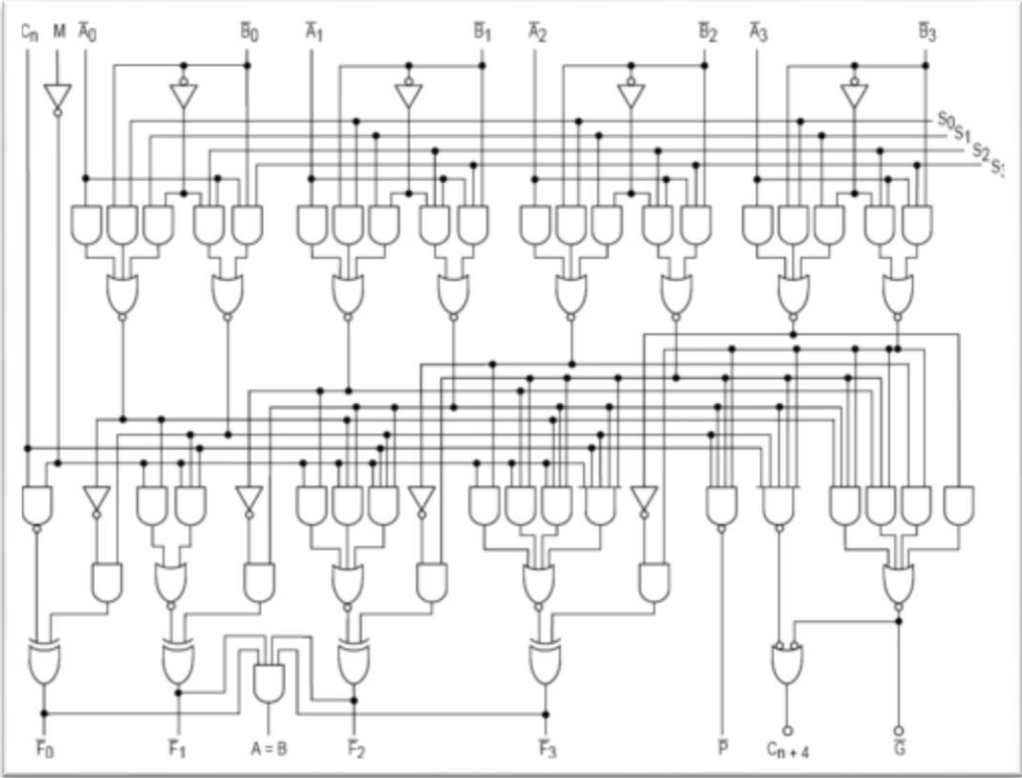
4 bits of ALU

Reset Circuit

+5Volt

Switch

C

To RESET IN

10μF

Ground

CLOCK Circuit

X1

X2

C1

C2

☐ INTR (Input)   Interrupt Request: This is used as a general-purpose interrupt; it is similar to the INT signal of the 8080A.

☐ INTA (Output)   Interrupt Acknowledge: This is used to acknowledge an interrupt.

☐ RST 7.5 (Inputs)   Restart Interrupts: These are vectored interrupts that transfer the program control to specific memory locations. They have higher priorities than the INTR interrupt. Among these three, the priority order is 7.5, 6.5, and 5.5.
   RST 6.5
   RST 5.5

☐ TRAP (Input)   This is a nonmaskable interrupt and has the highest priority.

| Pin	Subroutine Location
TRAP	0024
RST 5.5	002C
RST 6.5	0034
RST 7.5	003C
INTR	*
Note: * the address of the ISR is determined by the external hardware.	

Demultiplexing of AD_0-AD_7 :
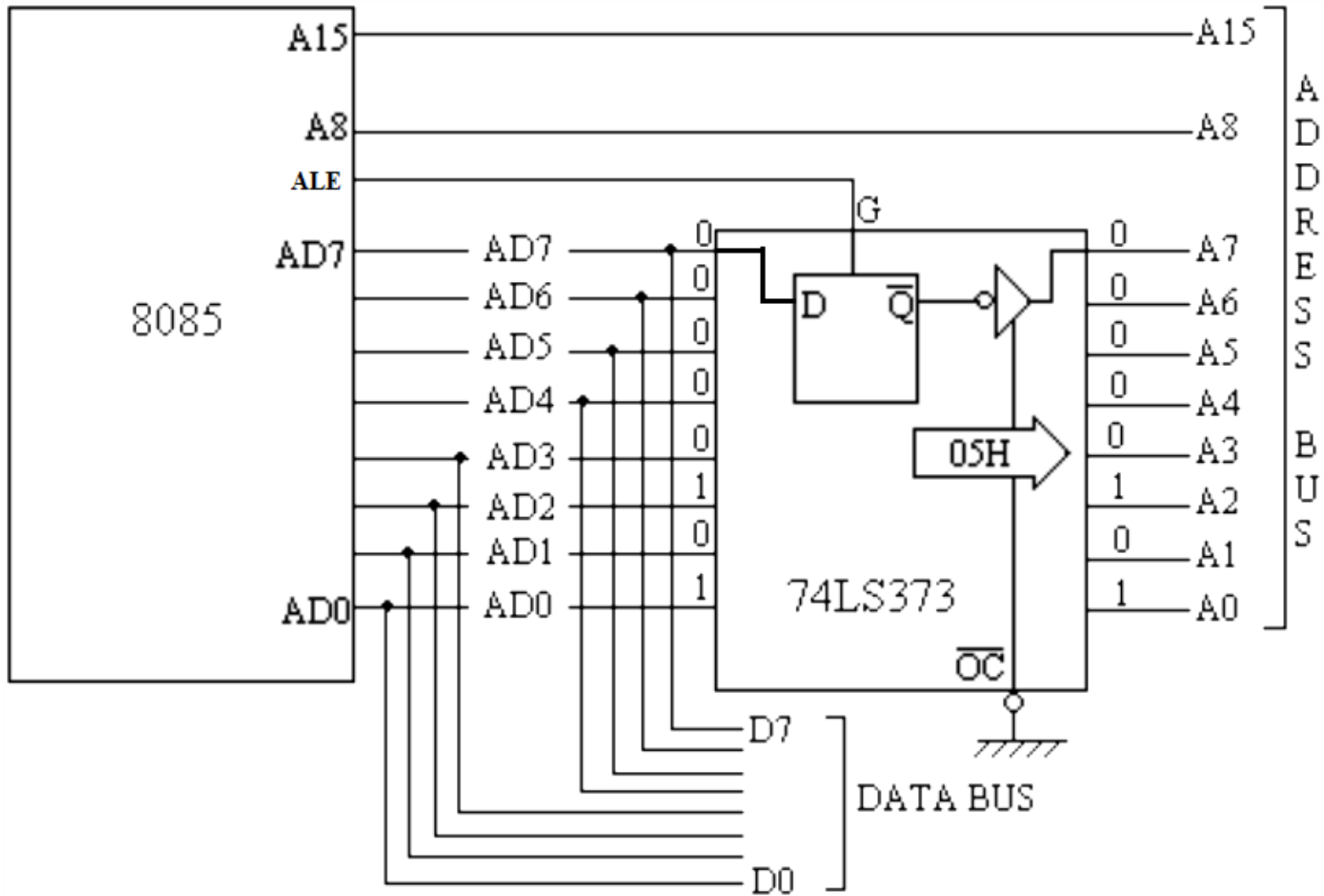
8085 Machine Cycles :

The 8085 microprocessor has 5 (five) basic machine cycles as shown in Table 1.2.

| Machine cycle	Status signals			Control signals	
	IO/M	S1	S0	RD	WR
1. Opcode fetch cycle (4T)	0	1	1	0	1
2. Memory read cycle (3 T)	0	1	0	0	1
3. Memory write cycle (3 T)	0	0	1	1	0
4. I/O read cycle (3 T)	1	1	0	0	1
5. I/O write cycle (3 T)	1	0	1	1	0

Interfacing Memory:

-              Select the chip.
    - •Identify the memory register.
    - •Enable the appropriate buffer.
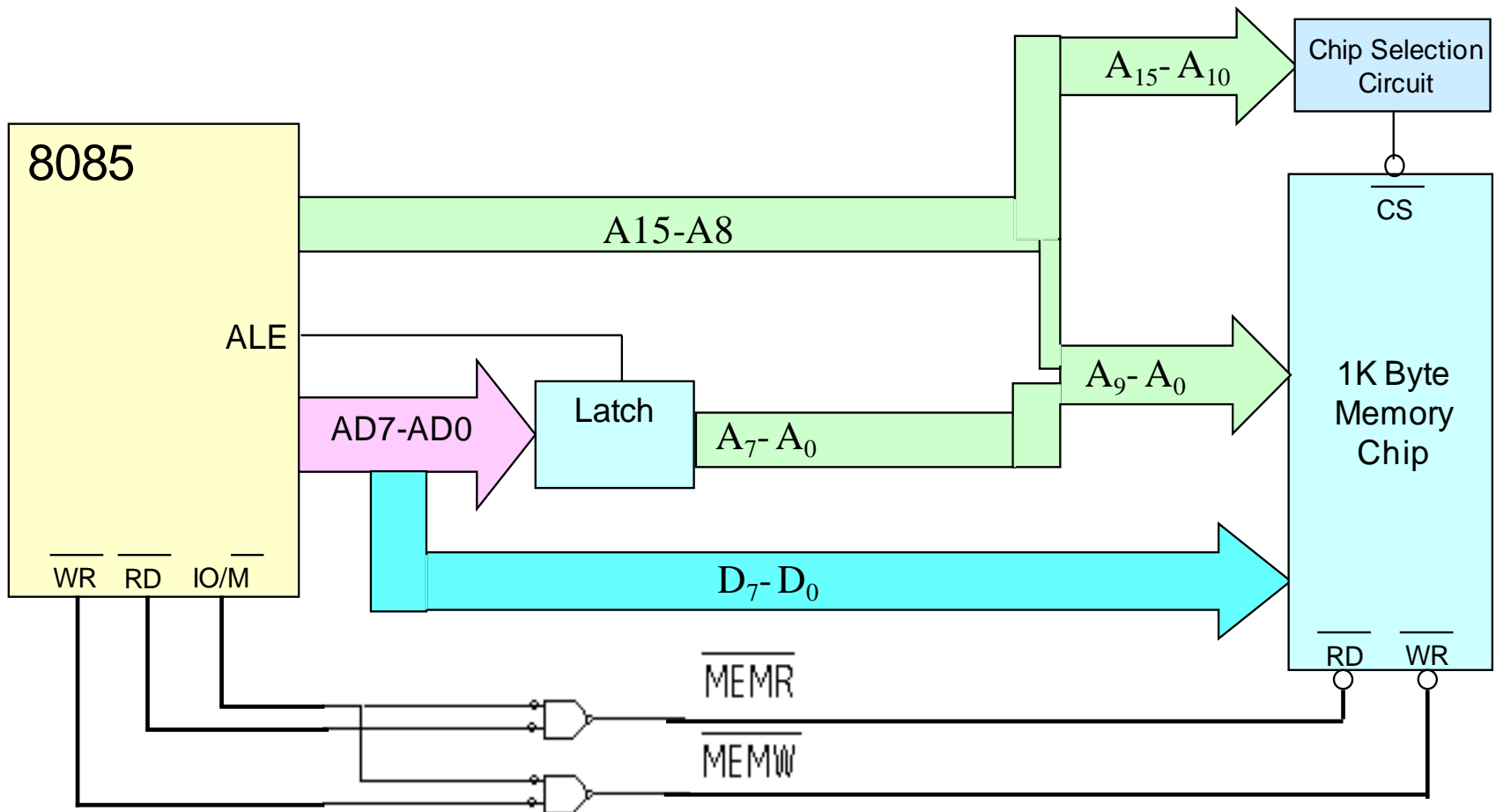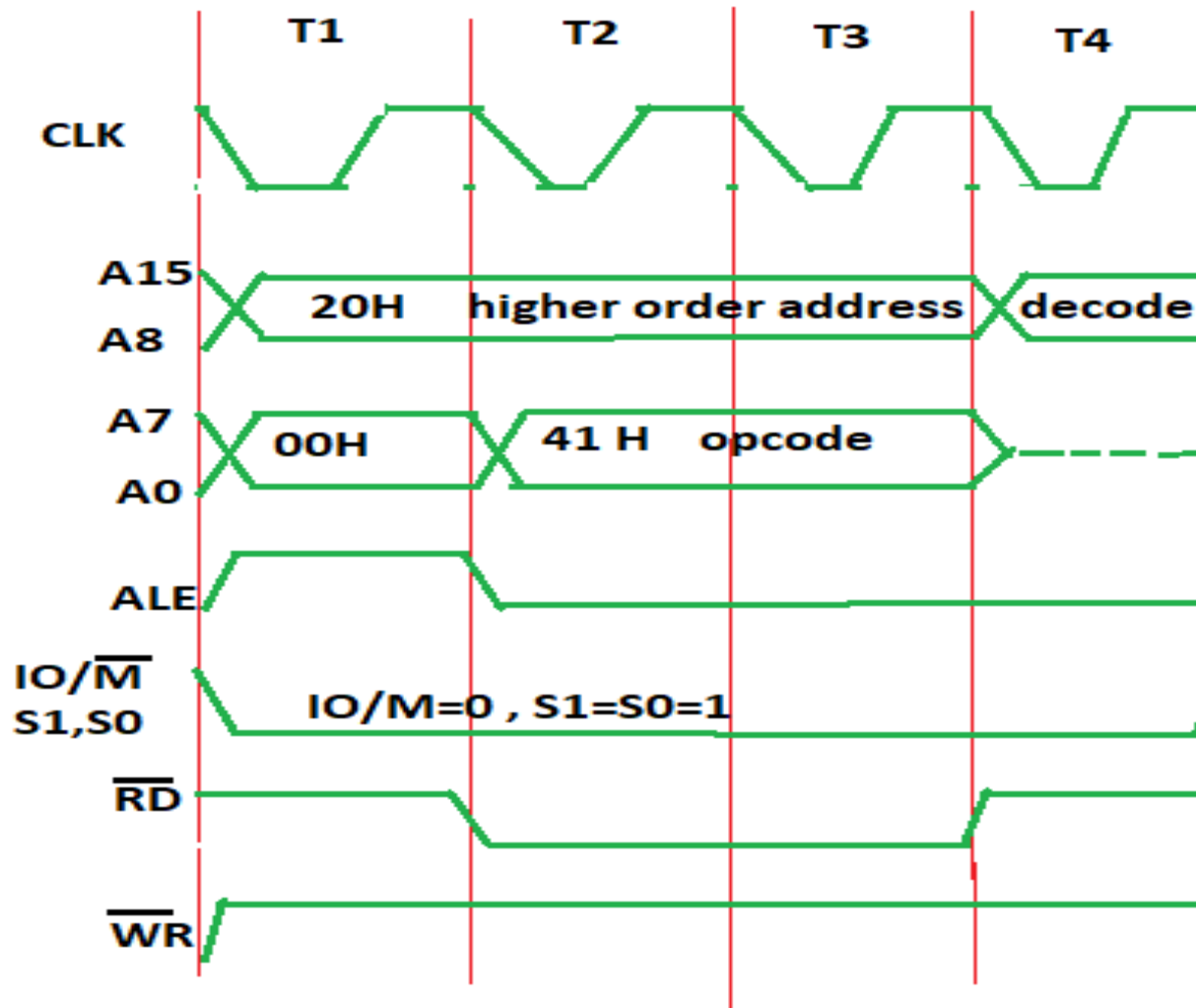
Timing diagram of MOV Instruction

Address	Hex Codes	Mnemonic	Comment
2004	5C	MOV E, H	E <- H
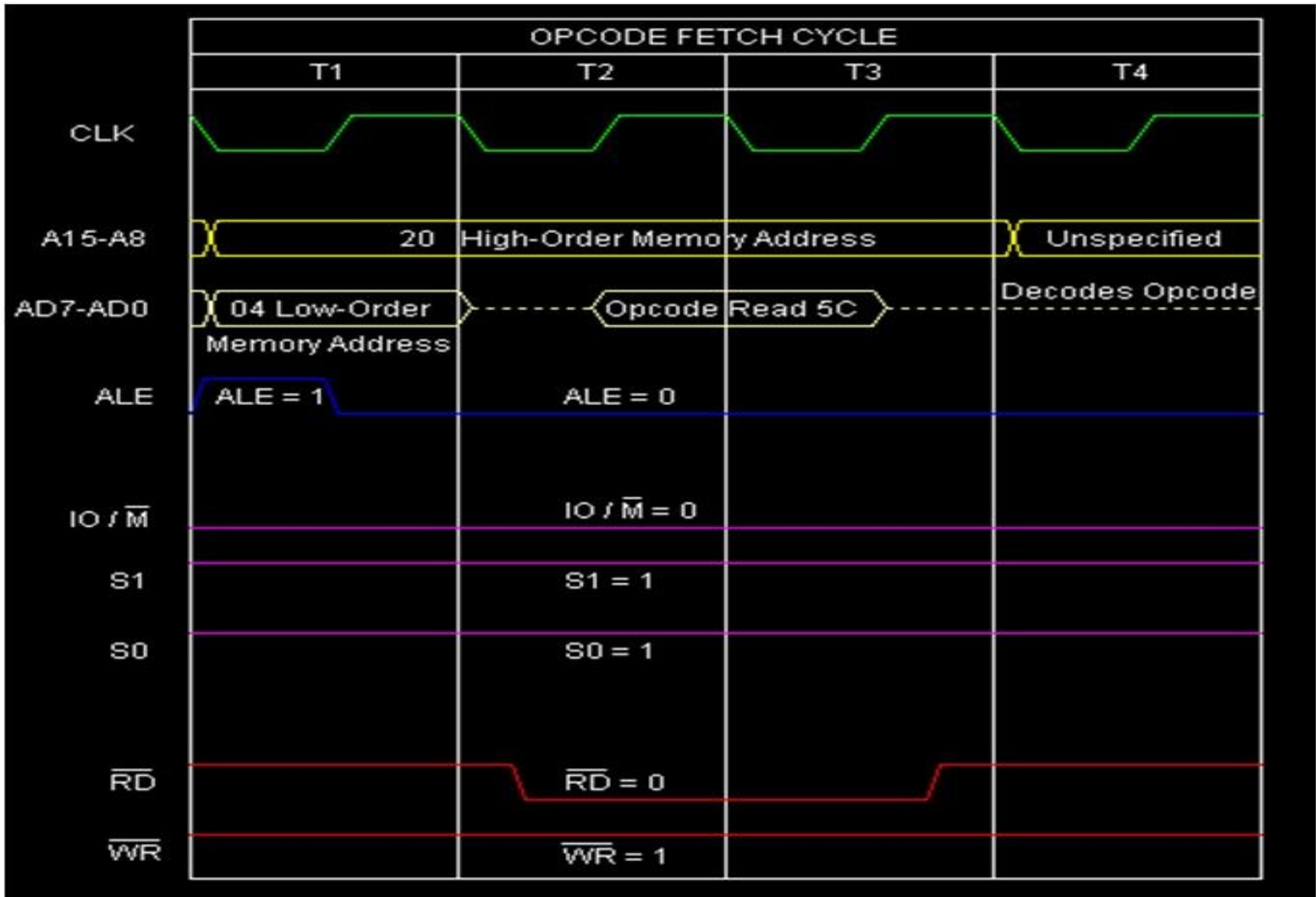
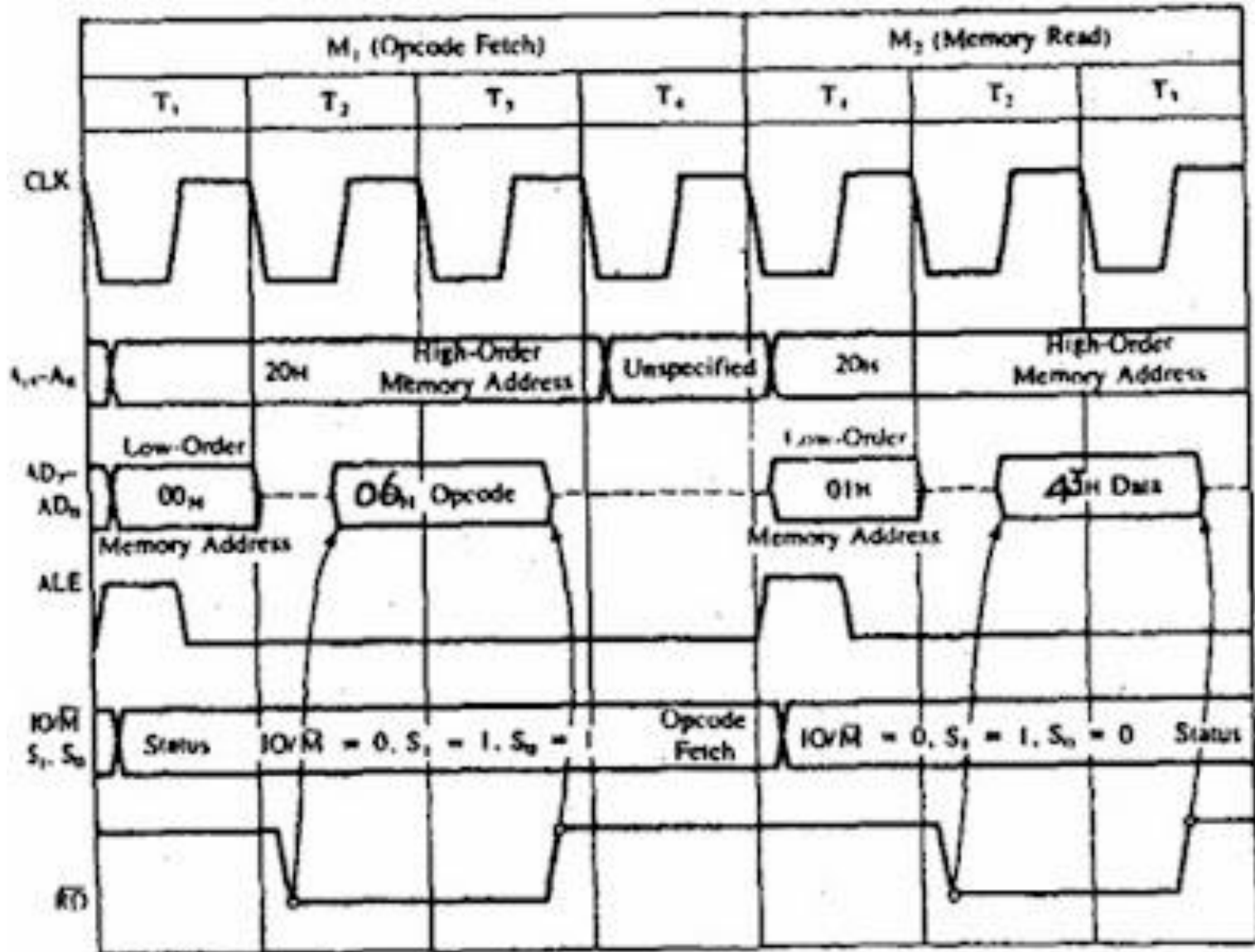# Timing diagram of MOV Instruction

`2000:  MOV  B,  C` copies the contents of the source register into the destination register
The instruction MOV B, C is of 1 byte; therefore the complete instruction will be stored in a single memory address

Address	Mnemonics	Opcode
2000	MVI B, 43$_H$	06$_H$
2001		43$_H$

Timing diagram of MVI Instruction

Select correct alternatives:
1) 8085µp is ------- bit microprocessor.
    a) 4   b) 8   c) 16   d) 32
2) Operating frequency of 8085µp is -------MHz
    a) 1   b) 2   c) 3   d) 4
3) ------ technology is used to fabricate 8085µp.
    a) NMOS   b) CMOS c) HMOS d) TTL
4) ------ register is used to indicate status of the result.
    a) ACC   b) Flag   c) PC   d) SP
5) ------is a 16 bit register.
    a) ACC   b) Flag   c) PC   d) B
6) ----- is a memory pointer register.
    a) ACC   b) Flag   c) PC   d) B
7) ------ signal is used to Demultiplexing AD0-AD7.
    a) RESET IN   b) ALE   c) S0, S1 d) IO/M
8) 8085 microprocessor can access ------- bytes of memory.
    a) 8 K   b) 16K   c) 32K   d) 64K
9) 8085 microprocessor has ----- bit data bus.
    a) 4   b) 8   c) 16   d) 32
10) To communicate with slower memories ------- signal is used.
    a) RESET IN   b) ALE   c) READY d) HOLD

11. --------are 16-bit registers.

a) PC and ACC   b) SP and ACC   c) PC and SP d) ACC and B

12. ---------------is not be an Interrupt signal.

a) INTR   b) RST 7.5   c) RST 5.5   d) HOLD

13. Principal register in 8085 microprocessor is------

a) ACC   b) Flag   c) PC   d) SP

14. ------------------registers can be acts as inputs for ALU.

a) ACC and B b) B and C   c) PC and SP d) ACC and Temp Register

15. ------------------registers are not user accessible.

a) ACC and B b) B and C   c) PC and SP d) W and Z

16. 8085 microprocessor has-----------number of General purpose registers.

a) 4   b) 6   c) 8   d) 10

17. 8085 microprocessor has------it address bus.

a) 4   b) 8   c) 16   d) 32

17. 8085 microprocessor can be reset by using --------signal.

18.HOLD   b) ALE   c) READY   d) RESET IN

19. If crystal of 6MHz is connected to Microprocessor then the operating clock frequency is—

MHz   a) 6   b) 3   c) 16   d) 1

20. Microprocessor writes a data into a memory by activating the signals as--------

        a) S0=0, S1=0, IO/M=1, RD=0   b) S0=0, S1=0, IO/M=0, RD=0

        c) S0=0, S1=1, IO/M=0, WR=0   d) S0=1, S1=0, IO/M=0, WR=0

21. Microprocessor reads a data from input device by activating the signals as--------

        a) S0=0, S1=0, IO/M=1, RD=0   b) S0=0, S1=0, IO/M=0, WR=0

        c) S0=0, S1=1, IO/M=0, WR=0   d) S0=0, S1=1, IO/M=1, RD =0

22. ----------signal is not an output signal.

      a)   RD   b) WR   c) S0   d) READY

23. Microprocessor uses-----------signals to communicate with serial devices.

    a)   HOLD and HLDA   b) TRAP and RST 7.5   c) SID and SOD   d) READY and HOLD

24. Addressing capacity of microprocessor depends upon--------

    a)   address lines   b) data lines   c) control lines   d) all of these

25. 8085 microprocessor has primarily------------interrupt signals.

        a) 4   b) 5   c) 8   d) 10

26. The 8085 microprocessor uses------signals to share system bus with Direct Memory Access (DMA) controller.

    a)   HOLD and HLDA   b) TRAP and RST 7.5   c) SID and SOD   d) READY and HOLD