"Dissemination of Education for Knowledge, Science and Culture"
-Shikshanmaharshi Dr. Bapuji Salunkhe

Shri Swami Vivekanand Shikshan Sanstha, Kolhapur

Vivekanand College, Kolhapur (Autonomous)

Department of Physics

B.Sc. Part- III

Semiconductor Devices and Instrumentation

Surprise Test

Date : 03/02/2023 **Total Marks: 20**

Day: - Friday **Time :- 2pm to 3pm**

Instructions:-

1) All questions are compulsory.
2) Figures to the right indicate full marks.
3) Use of log table and calculator is allowed.

Q1) Select correct alternative. **(05)**

1.In IC 555, reference voltage at trigger terminal is ……

a) Vcc b) 2/3Vcc c) 1/3 Vcc d) 2Vcc

2. The discharge time constant in iC 555 astable multivibrator is …….

a) $(R_a + R_b)\,C$ b) $R_a\,C$ c) $R_b\,C$ d) $(R_a - R_b)\,C$

3. The rms value is obtained by dividing peak voltage by …….

a) 2 b) $(2)^{1/2}$ c) 3 d)4

4. An AC signal of frequency 100 Hz is applied to X input and that of unknown frequency is applied to Y input of the C'RO gives I vertical and 5 horizontal loops in Lissajous figure is obtained on the screen, then the unknown frequency is …….Hz

a) 200 b) 300 c) 400 d)500

5. An unknown AC voltage is given to vertical input of CRO, the V_{peak} equal to 40 mV, V_{rms} = …….mV

a) 28.3 b) 0.28 c) 283 d) 40

Q 2: Long answer question (any one) **(10)**

1.. Draw the circuit diagram of monostable multivibrator using IC 555 explain its working and draw waveforms obtain an expression for frequency of oscillation.

2. Draw block diagram of IC 555 explain the working of IC 555 timer

Q 3: Short answer question (any one) **(05)**

1. Draw pin configuration of IC 555 and explain the function of each pin.

2. Obtain an expression for frequency or oscillation and duty cycle of astable multivibrator using IC 555.

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Vivekanand College, Kolhapur (Autonomous)

Department of Physics

B.Sc. III

Semiconductor Devices and Instrumentation

Surprise Test

Attendance Sheet

Date : 03/02/2023

Roll. No.	Name of Candidate	Sign
8201	Dhiraj Prakash. B	
8209	Tejas Y. Kothavale	TKothavale
8204	Abhishek. D.	
8203	Sujash Dongaee	Dongaee
8208	Anjali bhagwan. k.	
8206	Jayant Y. Naradekar	Jayant
8202	Prathamesh Dongaee	PDongaee
8213	Vivek Shelole	
8807	Shubham Kulkarni	
8214	Aishwarya Dipak Shingade	
8210	Aman I. Maner	
8217	Vedaja A. Yadav	
8216	Shriyansh K. Wakare	
8212	Aaban P. Patil	

Teacher Incharge..... Shinde

(Mr. A. V. Shinde)

VIVEKANAND COLLEGE KOLHAPUR ESTD JUNE 1964 (Autonomous)

Chamble

Head of the
Department of Physics
Vivekanand College, Kolhapur

"Dissemination of Education for Knowledge, Science and Culture"
-Shikshanmaharshi Dr. Bapuji Salunkhe

Shri Swami Vivekanand Shikshan Sanstha, Kolhapur

Vivekanand College, Kolhapur (Autonomous)

Department of Physics

B.Sc. III

Semiconductor Devices and Instrumentation

Surprise Test

Result

Date : 03/02/2023

Roll. No.	Marks	Roll. No.	Marks
8201	17	8225	–
8202	–	8226	–
8203	08		
8204	15		
8205	–		
8206	18		
8207	09		
8208	20		
8209	07		
8210	11		
8211	–		
8212	10		
8213	12		
8214	09		
8215	–		
8216	10		
8217	12		
8218	–		
8219	–		
8220	–		
8221	–		
8222	–		
8223	–		
8224	–		

Teacher Incharge..... ShindeAV

(Mr. A.V. Shinde)

VIVEKANAND COLLEGE KOLHAPUR ESTD JUNE 1964 (Autonomous)

Ckamble

Head of the
Department of Physics
Vivekanand College, Kolhapur.

Dhiraj Prakash Bhingardeve

27382

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VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

SUPPLIMENT

Signature of Supervisor	

Suppliment No. :

Roll No. : 8201

Class : BSc-III

Subject : Semiconductor devices & instrumentation

Test / Tutorial No. : 17

Div. : /20

Q.1

1) In IC 555, reference at trigger terminal is → c) 1/3 Vcc

2)

→ a) $(R_A + R_B)C$

3)

→ b) $\sqrt{2}$

4)

→ a) 200

5)

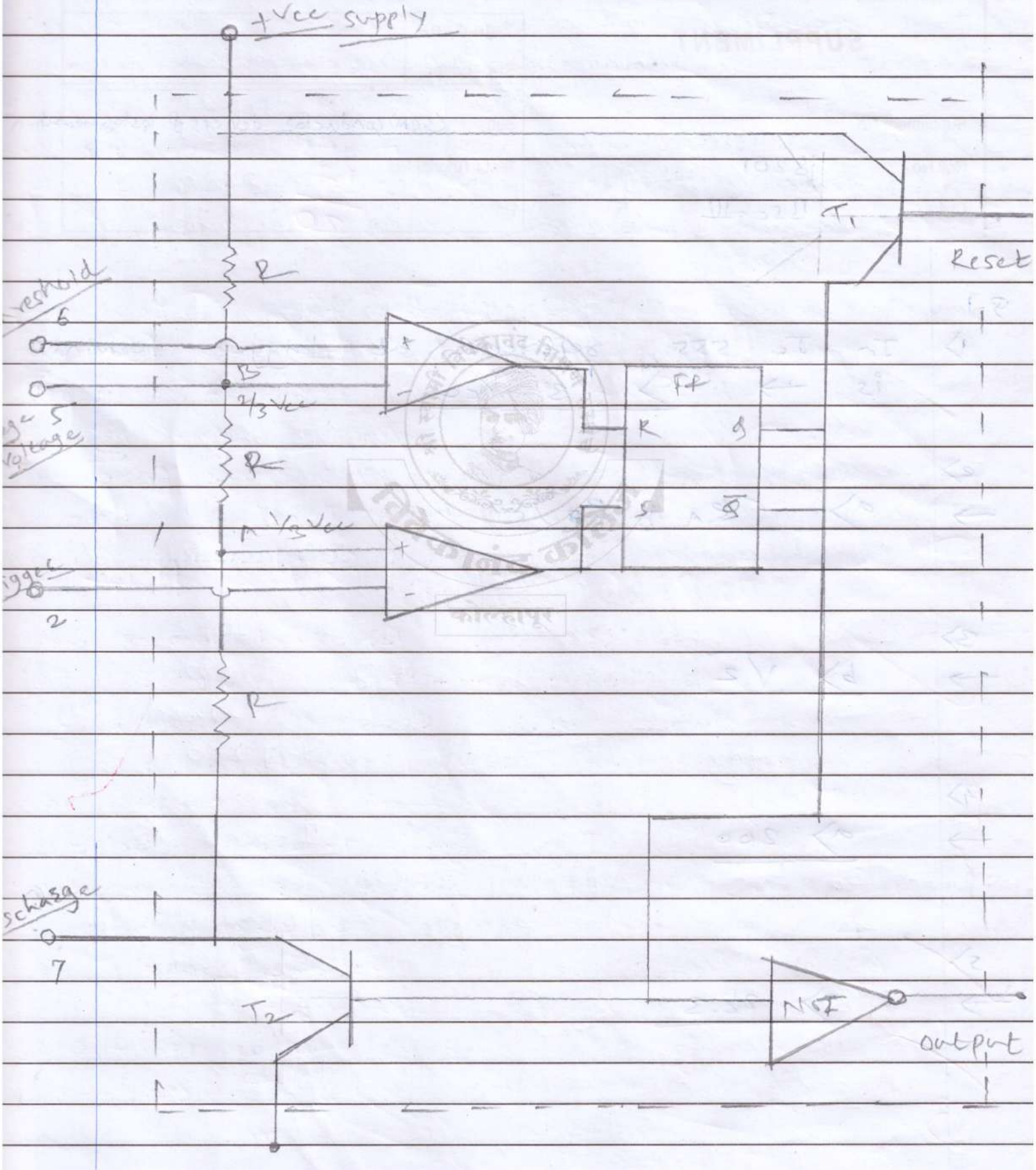
→ a) 28.3

3

Q.2

2)

→


+Vcc supply
R
R
R
Threshold
6
B
2/3 Vcc
A
1/3 Vcc
Trigger
2
Discharge
7
T1
Reset
FF
R
Q
S
NOT
output
T2

1) The timer Ic 555 is an integrated circuit having timer and multivibrator applications. The timer Ic 555 is 8- pin configuration circuit. it is the one of the most versatial sequential digital logic circuit. at past from the application of multivibrator as ?- Timer Ic 555 it can be used to Dc- Dc converstores digital logic waveforms generator.

2) the Ic 555 ~~is~~ has (2) Comparator which basically (2) op-amps, a flip. Flop, (2) Transistores and Resistive network. Resistive network consist equal (3) Resistores, and this resistores are acts like voltage Divider. due to this voltage at point (A) lowes voltage as at a point (B).

(3) Ic 555 is (2) Comparatores which is operational amplifiers, as flip-flops transistores and Resistence network & inverter (not gate). Resistance are voltage divider, then the output of Comparator I ~~Trigge~~ Compares Threshold voltage $2/3$ Vcc and output of Comparator II compares trigger voltage $1/3$ Vcc.

(4) + Vcc is the voltage supply it energised the circuit. the Comparator I compares threshold voltage is $2/3$ Vcc & comparator II compares trigger voltage is $1/3$ Vcc.

then output of Comparator I is (R) input and output of Comparator II is (S) input. R-S Flip Flop. in a state Comparator and Transistor connected to and Collector is connected to between this terminal and capacitor is Discharge transmitter. whose Collector is connected to the Discharge Voltage (Pin 7) through lower end of the resistance network.

* Work of Ic 555 is summerised on some cases.

1) Case I:

when no trigger and Threshold Voltage applied then Comparator II is high (1) and Comparator - I is low then

S = 1, R = 0, then set in state

Q = 0 $\bar{Q}$ = 1

hence,

output of times is high.

2) Case-II

when trigger pulse of negative Voltage is greater than 1/3 Vcc than

S = 0, Q = 0 and $\bar{Q}$ = 1

hence,

output of times is low

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– शिक्षणमहर्षी डॉ. बापूजी साळुंखे
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VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

SUPPLIMENT

Signature of Supervisor: 15/20

Suppliment No. :

Roll No. : 8204

Class : BSc-III

Subject : Physics

Test / Tutorial No. : Internal Exam

Div. :

1

1 1/3 Vcc

2 RBC

3 $\sqrt{2}$

4 500 Hz

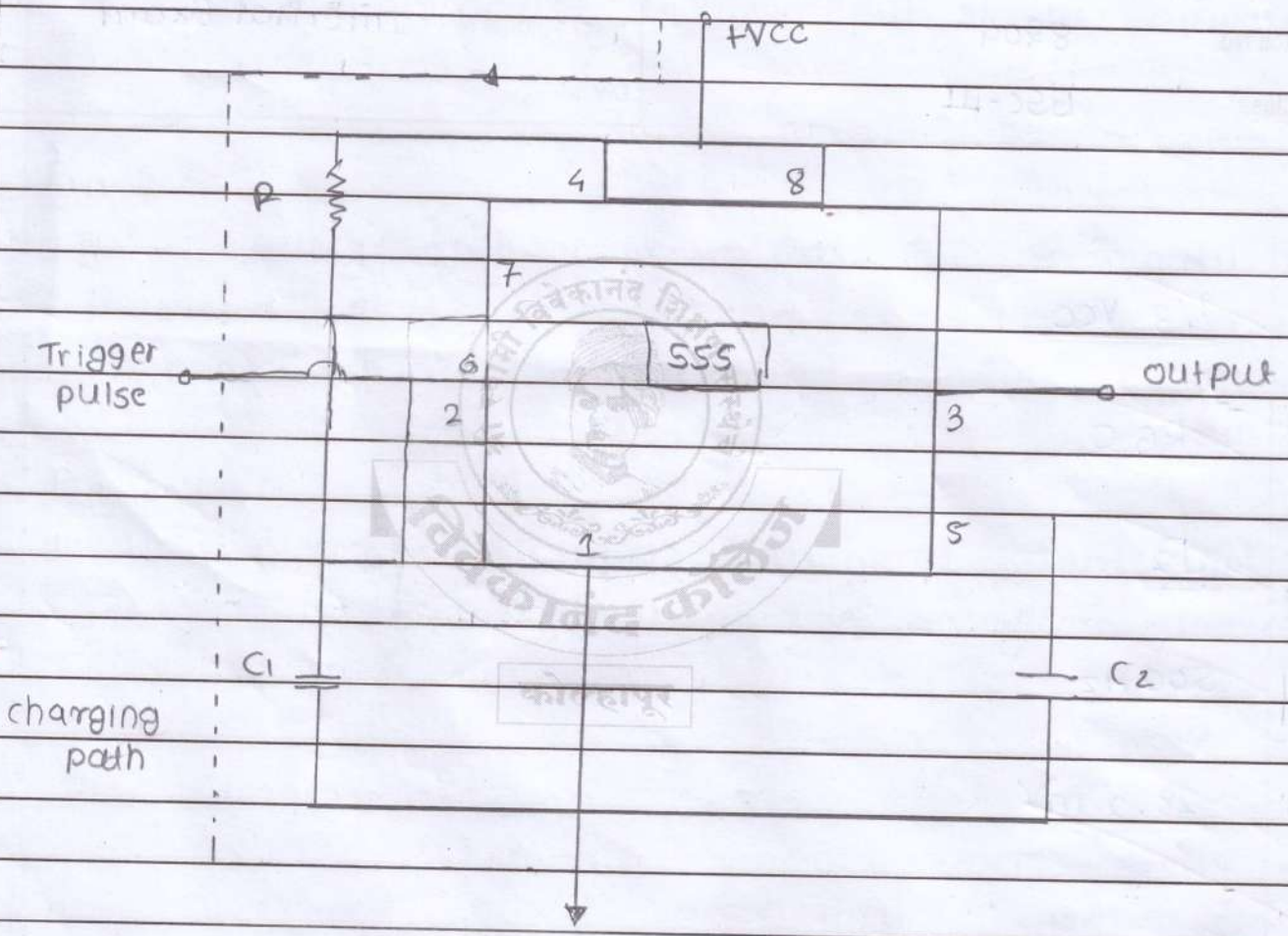
5 28.2 mV

5

Q. 2

ii) Monostable Multivibrator

- The multivibrator has one stable state .so it is named as monostable multivibrator
- The circuit is allowed unstable state.



Block diagram of Monostable multivibrator

From above Fig Block diagram of monstable timer IC-555 the Resistance R is connected to Pin 4 Pin 6 Pin 7 and Pin 8 the capacitor C is connect to Pin 6 and 7 and ground. trigger pulse is connected to Pin 2 Pin 1 is Grounded and Pin 5 giving trough capacitor output is taken at Pin 3 and Pin 4 is goes through +Vcc.

Q. 2

i] Monostable Multivibrator

- The multivibrator has one stable state .so it is named as monostable multivibrator
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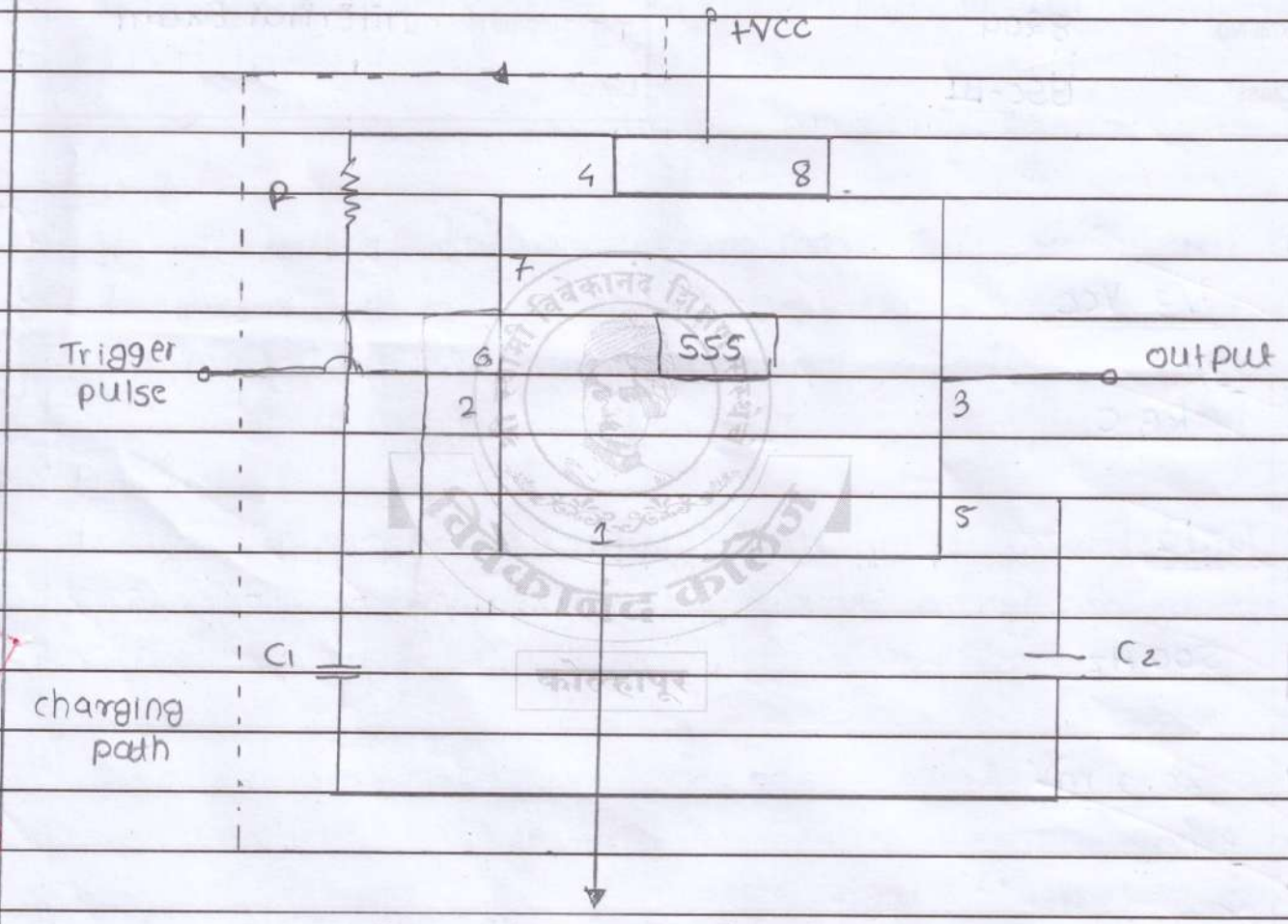

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The switching voltage level of comparator 1 is decided by the voltage at this terminal and thus it changes the pulse width of the output

Pin 6 -

This is threshold terminal It forms the non-inverting terminal of comparator 1 the output of this comparator is low

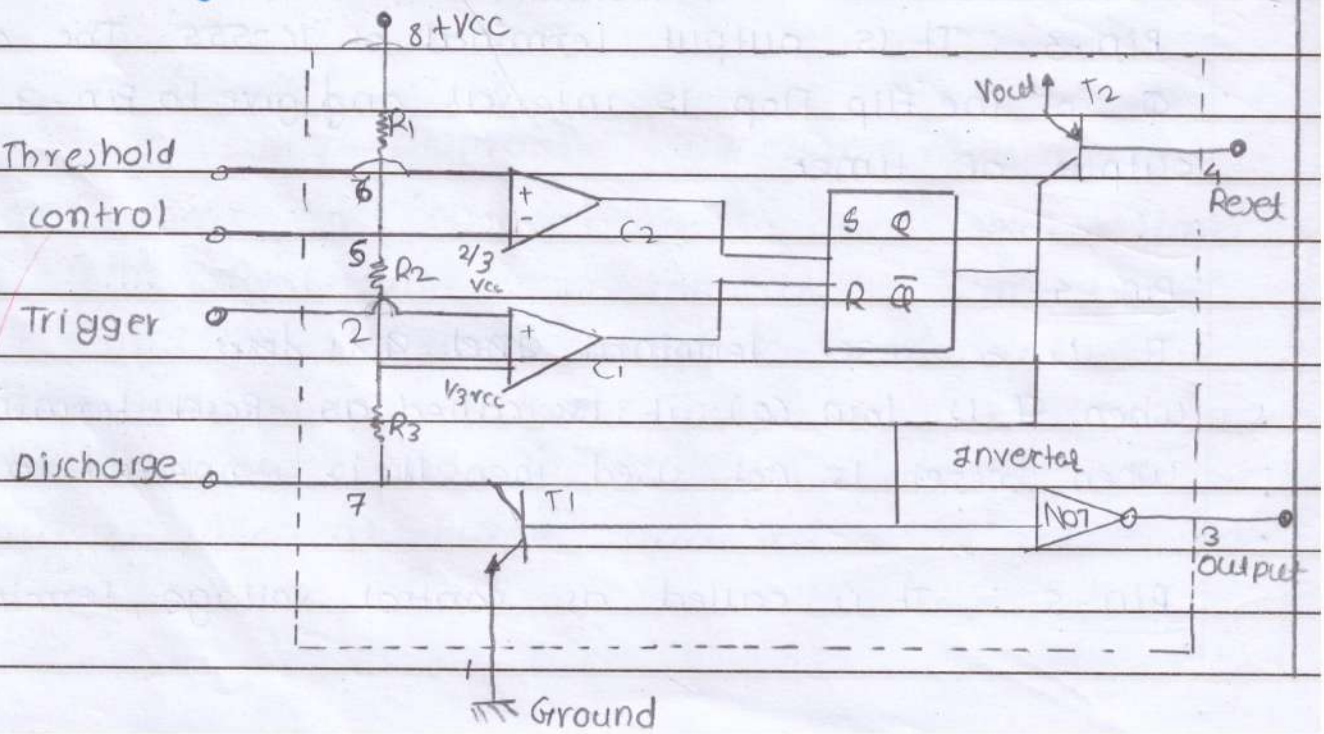
Pin 7 :

It is called discharge terminal. This terminal is intern Connected to the collector and transistor T_2 and a inpu is connected between terminal and ground

Pin - 8

It is called as a supply voltage terminal. The voltage of this terminal provides energy through the circuit.

Q.2 (2) Block diagram of Timer IC - 555



Mahek S Jamadar

।। ज्ञान, विज्ञान आणि सुसंस्कार यांसाठी शिक्षण प्रसार ।।

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VIVEKANAND COLLEGE, KOLHAPUR (AUTONOMOUS)

SUPPLIMENT

Signature of Supervisor	18/20

Suppliment No. :

Roll No. : 8206

Class : BSc III

Subject : Semiconductor Devices & instrumentation

Test / Tutorial No. : Internal Exam

Div. :

1) c) 1/3 V_{CC}

2) a) $(R_A + R_B)C$

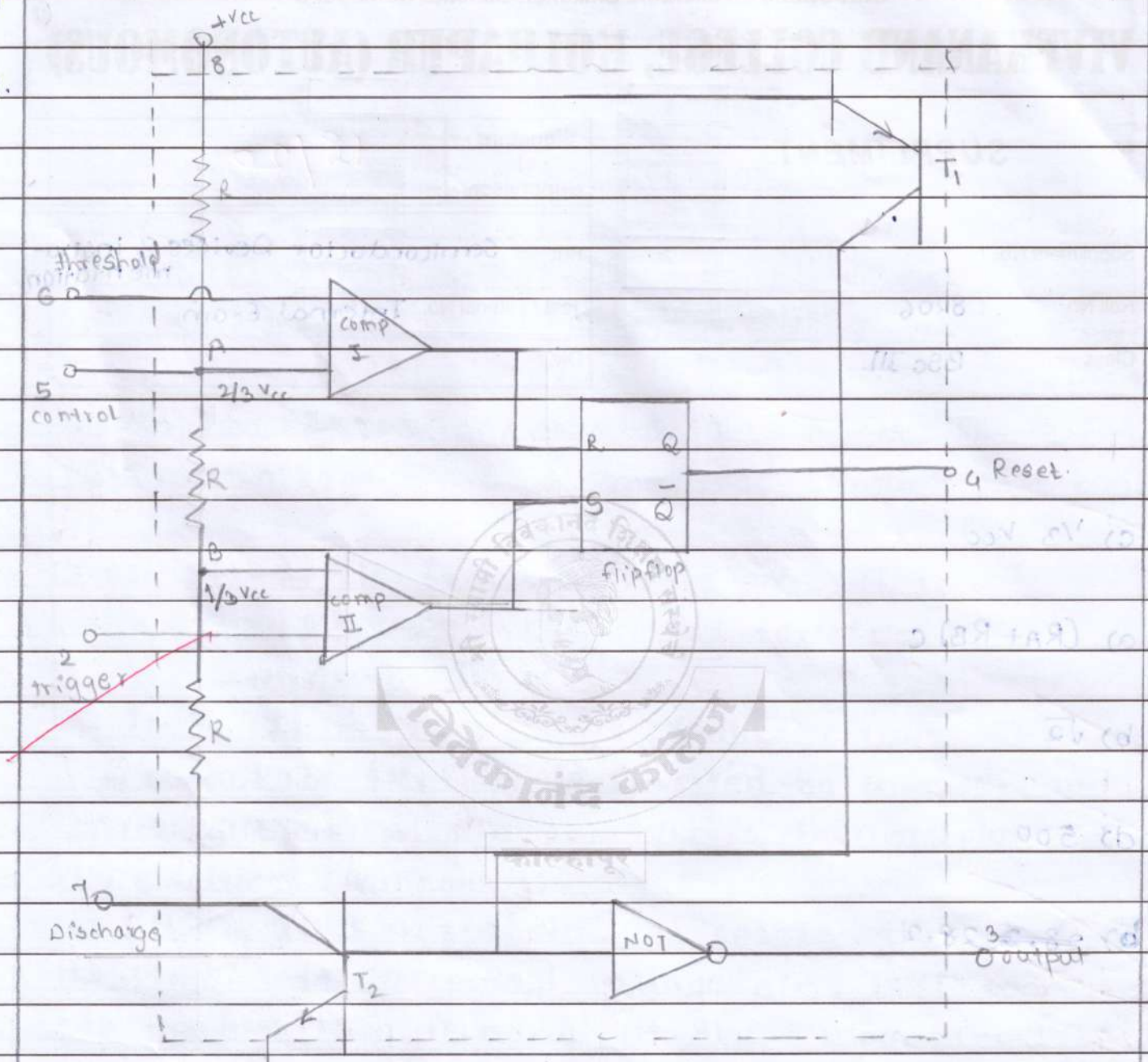
3) b) $\sqrt{2}$

4) d) 500

5) b) ~~28.2~~ 28.2

22]

2.



IC 555 is an integrated circuit. The block diagram contains various electronic components within it. It consists of two comparators (operation amplifiers) two transistors T_1 & T_2, NOT gate inverter and a resistive network R. Resistive network R is a network of three equal resistances. It is a voltage dividing network of supply of voltage V_{cc}. The supply voltage energises the circuit.

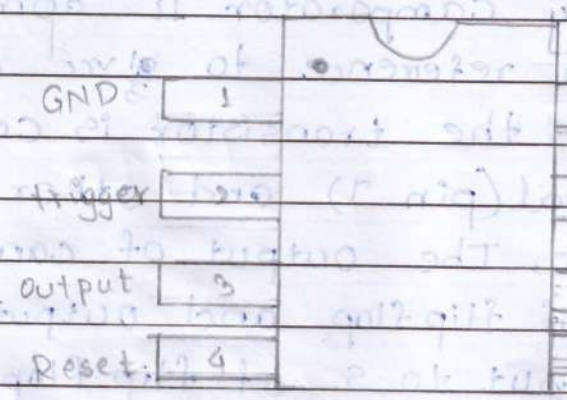
Comparator I compares the ~~output~~ threshold voltage with reference to control voltage at point A. Similarly Comparator II compares trigger voltage with reference to $\frac{1}{3}V_{cc}$ at pt. B. The collector of the transistor is connected to discharge terminal (pin 7) and other end is grounded to (pin 1). The output of comparator I is input to R of flip flop and output of comparator II is input to S of flip flop. The ~~NOT~~ Gate is an inverter i.e it inverts the output of flipflop and gives output of circuit to output terminal (pin 3). The reset terminal (pin 4) resets the circuit.

The stepwise working of block diagram can be explained as follows:
When T_1 is set on then the output goes to two ends - one to the input of NOT gate and other ~~to~~ T_2. When threshold voltage exceeds $\frac{2}{3}V_{cc}$ the circuit is reset and the output $\bar{Q}$ is high. Hence the output of timer is low. ~~This~~ This is set state and it continues till the trigger is applied. When trigger is applied to comparator II the value exceed the $\frac{1}{3}V_{cc}$ voltage and $\bar{S}$ becomes high. The output of flipflop at $\bar{Q}$ therefore becomes low. This output is inverted and output of the timer at pin 3 is high.

The reset terminal resets the circuit irresp of an input given.

Q3]

1)



1) Pin 1: It is connected to ground. The supply voltage +Vcc is grounded through this pin.

2) Pin 2: It is trigger ~~termin~~ pin. It gives input to ~~co~~ noninverting terminal of comparator II.

3) Pin 3: It is output pin of the circuit. The $\bar{Q}$ output of flipflop is inverted by inverter and gives output at pin 3 which is then displayed by electronic components.

4) Pin 4: It is reset pin. It resets the flipflop.

5) Pin 5: It is control voltage pin. It is connected to noninverting terminal of the comparator I.

6) Pin 6: It is threshold pin. It is connected to inverting terminal of comparator I.

pin 7: It is discharge terminal. It is connected to collector of transistor and discharge voltage takes place through this.

8) Pin 8: ~~Vo~~ Voltage supply to whole circuit is given through this pin.

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SUPPLIMENT

Signature of Supervisor	14/20

Suppliment No. :

Roll No. : 8210

Class : Bsc III

Subject : Semiconductor devices and instrumentation

Test / Tutorial No. : Internal exam

Div. :

Q1

1) In IC 555, reference voltage at trigger terminal is
a) 1/3 Vcc

2) The discharge time constant in IC555 astable multivibrator is a) $(R_A + R_B)C$

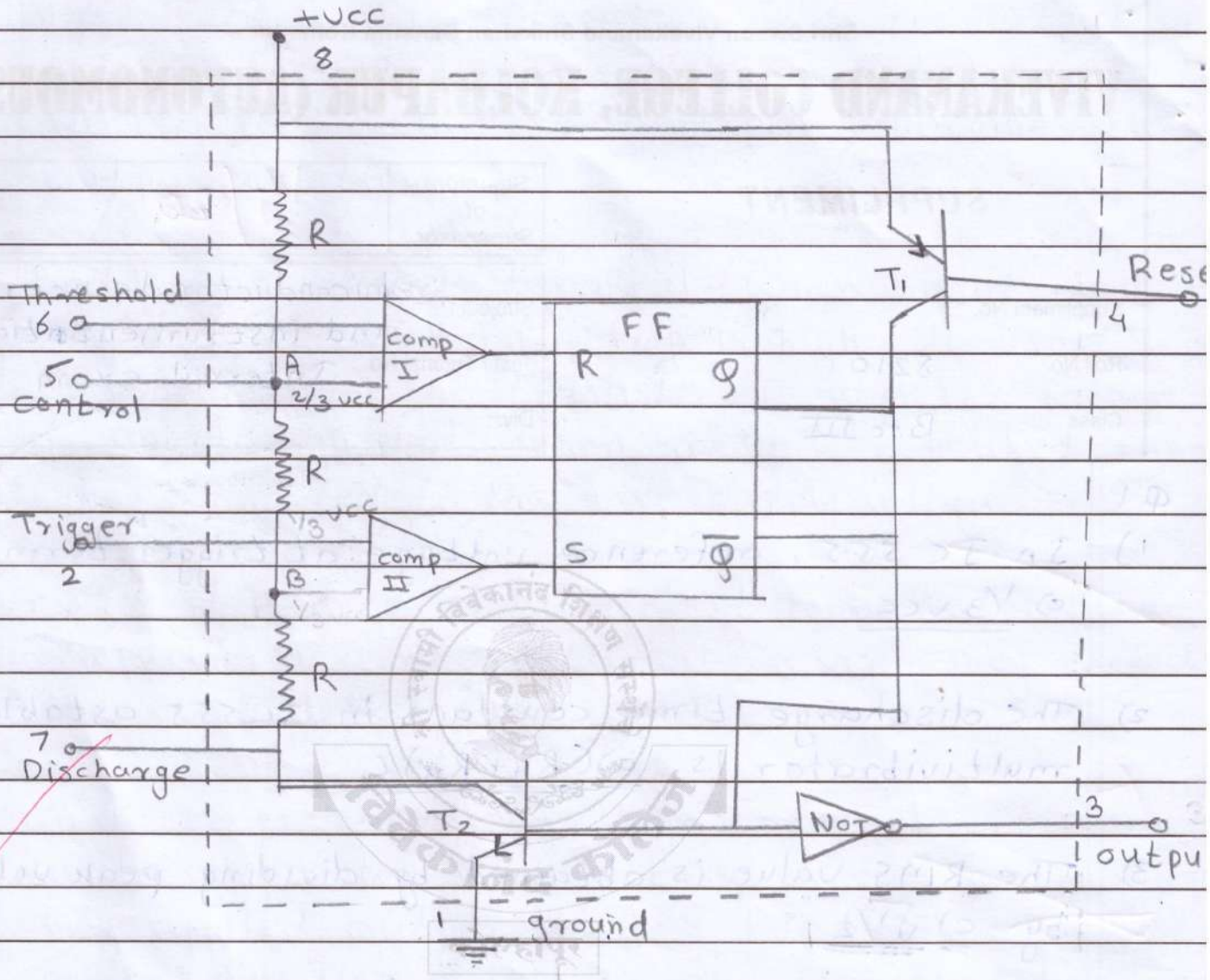
3) The RMS value is obtained by dividing peak voltage by c) $\sqrt{1/2}$

4) d) 500 Hz

5) An unknown AC voltage is given to vertical input of CRO, the Vpeak is equal to 40 mV, V_{rms} = 28.3 mV

Q2

2)



Working of IC Timer 555 are written as following cases.

Case I :-

When no threshold voltage applied to R-S flip flop then output of timer is high. Hence R=0 and S=1, Q=0, $\bar{Q}$=1

Case II :-

When trigger voltage applied less to 1/3 Vcc to R-S flip flop then S=0 and Q=1. So output of timer is low

Q 2

2)

→ Case III :-

When the threshold voltage applied greater than the 2/3 Vcc then R = 1 and Q = 1. So output of timer again becomes low.

Case IV :-

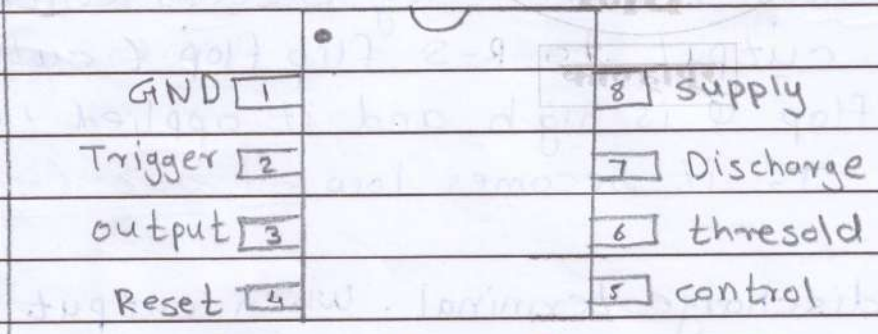
When Reset terminal is low then output of timer forces to high. Because when reset is not used then it is connect to the +Vcc supply voltage.

6

Q 3

1)

→



Pin confriguration of IC 555 are follows :-

Pin 1 :- It is a ground terminal. The voltage measured with respect to the ground terminal.

Pin 2 :- It is a trigger terminal. When trigger is applied to the R-S flip flop then output of timer becomes high. This timer is from ~~to~~ set to reset. They connected to the comparator II.

Q3

1) Pin 3 :- It is output terminal. When the output of R-S flip flop $\bar{Q}$ becomes high then it given to th NOT gate i.e. inverter and pin 3 becomes the output of timer.

Pin 4 :- It is reset terminal. When reset is low the output of R-S flip flop is high. Then output is provided to the transistor T_2 and it's become low and grounded. When reset is not used then they connected to the +Vcc supply voltage.

Pin 5 :- It is control voltage. It connected to the comparator I with voltage +2/3 Vcc. They exceeds the control the pulse width.

Pin 6 :- It is thresold voltage terminal. It connects to the comparator I when they exceeds control voltag They applied output to R-S flip flop & output of R-S flip flop $\bar{Q}$ is high and it applied to base of transistor T_2 it becomes low.

Pin 7 :- It is discharge terminal. When output of R-S flip flop is high then they applied to base of Transistor T_2 and it becomes low and grounded. It connected between transistor and ground.

Pin 8 :- It is ~~gre~~ voltage supply terminal. It provided voltage. It provide voltage to energies the circuit.